Basler A500k

USER'S MANUAL

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BASLER

For customers in the U.S.A.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

You are cautioned that any changes or modifications not expressly approved in this manual could void your authority to operate this equipment.

The shielded interface cable recommended in this manual must be used with this equipment in order to comply with the limits for a computing device pursuant to Subpart J of Part 15 of FCC Rules.

For customers in Canada

This apparatus complies with the Class A limits for radio noise emissions set out in Radio Interference Regulations.

Pour utilisateurs au Canada

Cet appareil est conforme aux normes Classe A pour bruits radioélectriques, spécifiées dans le Règlement sur le brouillage radioélectrique.

Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Basler customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Basler for any damages resulting from such improper use or sale.

Warranty Note

Do not open the housing of the camera. The warranty becomes void if the housing is opened.

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1 Introduction

BASLER A500k area scan cameras are high speed CMOS cameras designed for industrial use. Good CMOS image sensing features are combined with a robust, high precision manufactured housing.

Important features are:

- CMOS APS (Active Pixel Sensor) technology
- High speed
- Electronic full frame shutter (True SNAP™ freeze-frame)
- Anti-blooming
- Electronic exposure time control
- Partial scan
- Programmable via an RS-644 serial port
- Industrial housing manufactured with high planar, parallel and angular precision
- VGA monitor output (**A504k/kc** only)
- Flash trigger output

1.1 Camera Versions

A500k series area scan cameras are available in different versions; the version depends on the maximum frame rate and on color or monochrome.

Throughout the manual, the camera will be called the **A500k**. Passages that are only valid for a specific version will be so indicated.

Camera Version	Max. Frame Rate	Monochrome / Color
A504k	500 fps	monochrome
A504kc	500 fps	color
A503k	402 fps	monochrome
A501k	74 fps	monochrome
A501kc	74 fps	color

Table 1-1: Versions of the **A500k** Series Camera

1.2 Performance Specifications

The image sensor characteristics were measured at 25°C.

Specifications	A504k	A504kc	A503k	A501k	A501kc
Sensor	1280 H x 1024 V pixel CMOS (1310720 pixels) Micron MV13 progressive scan				
	mono-chrome	color (see section 3.6)	mono-chrome	mono-chrome	color (see section 3.6)
Pixel Size	12 µm x 12 µm (12 µm pixel pitch)				
Fill Factor without micro lens	40%				
Sensor Imaging Area	H: 15.36 mm, V: 12.29 mm, Diagonal: 19.67 mm				
Digital Responsivity	See section 1.3 and Figure 1-1.	See section 1.3 and Figure 1-2.	See section 1.3 and Figure 1-1.	See section 1.3 and Figure 1-1.	See section 1.3 and Figure 1-2.
Shutter	Electronic full frame shutter: True SNAP™ (Shuttered-Node Active Pixel)				
Shutter Efficiency	99.9% (typical)				
Shutter Exposure Time	10 µs to greater than 33 ms				
PRNU (Photo Response Non-uniformity)	high spatial frequency: < 0.6 % rms (typical) low spatial frequency: < 10 % p-p (typical)				
DSNU (Dark Signal Non-uniformity)	high spatial frequency: < 0.4 % rms (typical) low spatial frequency: < 1.5 % p-p (typical)				
Vdrk (output referred dark signal)	75 LSB/s with digital shift = 0 (typical) 150 LSB/s with digital shift = 1 (typical) 300 LSB/s with digital shift = 2 (typical) 600 LSB/s with digital shift = 3 (typical)				
Kdrk (Dark current temperature coefficient)	+100% at + Δ 8°C				
Pixel Clock Speed	67.58 MHz			50 MHz	
Frame Rate	Max. 500 fps @ 1280 x 1024		Max. 402 fps @1280 x 1024 Max. 500 fps @ < 1040 x 1024	Max. 74 fps @1280 x 1024	
Output Data Rate	625 MBytes/s		502.5 MBytes/s	95 MBytes/s	
Pixel Depth	8 Bit out of 10				
Video Output Type	Channel Link® LVDS, 10 x 8 Data Bits		Channel Link® LVDS, 8 x 8 Data Bits	Channel Link® LVDS, 2 x 8 Data Bits	

Table 1-2: **A500k** Performance Specifications

Specifications	A504k	A504kc	A503k	A501k	A501kc
Video Output Format	10 taps 8 Bit each Camera Link® Full Configuration (Basler-specific bit assignment)		8 taps 8 Bit each Camera Link® Full Configuration	2 taps 8 Bit each; Camera Link® Base Configuration	
Synchronization	Via external ExSync signal or free-run				
Exposure Time Control	Edge-controlled, Level-controlled, or Programmable				
Gain and Offset	Programmable via the framegrabber via a serial link				
Connectors	All versions: 26 pin, 0.5“, mini D ribbon (MDR) plug (data) one 6 pin, Hirose HR (power) one 4 pin, Hirose HR (flash control) A504k/kc, A503k: second 26 pin, 0.5“, mini D ribbon (MDR) plug (data) A504k/kc: one 15 pin, high-density sub female (VGA monitor output)				
VGA monitor output	640 x 480 pixels at 60 Hz		-		
Power Requirements	12 VDC ± 10%; max 6 W		12 VDC ± 10%; max 5.4 W	12 VDC ± 10%; max 3 W	
Housing Size (L x W x H)	without connectors and lens adapter: 41.5 x 90 x 90 mm with connectors and F-mount adapter: 78.8 x 90 x 90 mm				
Lens Adapters	F-mount				
Weight without lens adapter: with F-mount adapter:	~ 510 g ~ 600 g			~ 520 g ~ 610 g	
Vibration	tested according to DIN IEC 60068-2-6 3 axes, x, y, z 5 - 8.5 Hz / 1.5 mm 8.5 - 150 Hz/ 10 m/s²				
Shock	tested according to DIN IEC 60068-2-27 3 axes, x, y, z 100 m/s², 11 ms, 3 shocks positive 100 m/s², 11 ms, 3 shocks negative				
Bump	tested according to DIN IEC 60068-2-29 100 m/s², 11 ms, 100 shocks positive 100 m/s², 11 ms, 100 shocks negative				
Conformity	CE, FCC				

Table 1-2: **A500k** Performance Specifications

1.3 Digital Responsivity

The specified digital responsivity is obtained if the **gain** is set to **98**. The values are valid for the monochrome chip. In addition, the output depends on the register setting for the digital shift. The values given are typical values which can vary between different cameras:

For digital shift = 0: 400 DN/lx s @ 550 nm

For digital shift = 1: 800 DN/lx s @ 550 nm

For digital shift = 2: 1600 DN/lx s @ 550 nm

For digital shift = 3: 3200 DN/lx s @ 550 nm

LSB = least significant bit

See section 3.7.1 for the formula.

Example:

If the gain is set to 98, if digital shift is set to 0, and the quantity of light of 1 lux-sec has hit the sensor, a gray value of 400 is output.

The quantum efficiency of the monochrome sensor is shown in Figure 1-1, and the quantum efficiency of the color sensor in Figure 1-2. The quantum efficiency of the color sensor is slightly lower than the quantum efficiency of the monochrome sensor. This is due to the color filter.

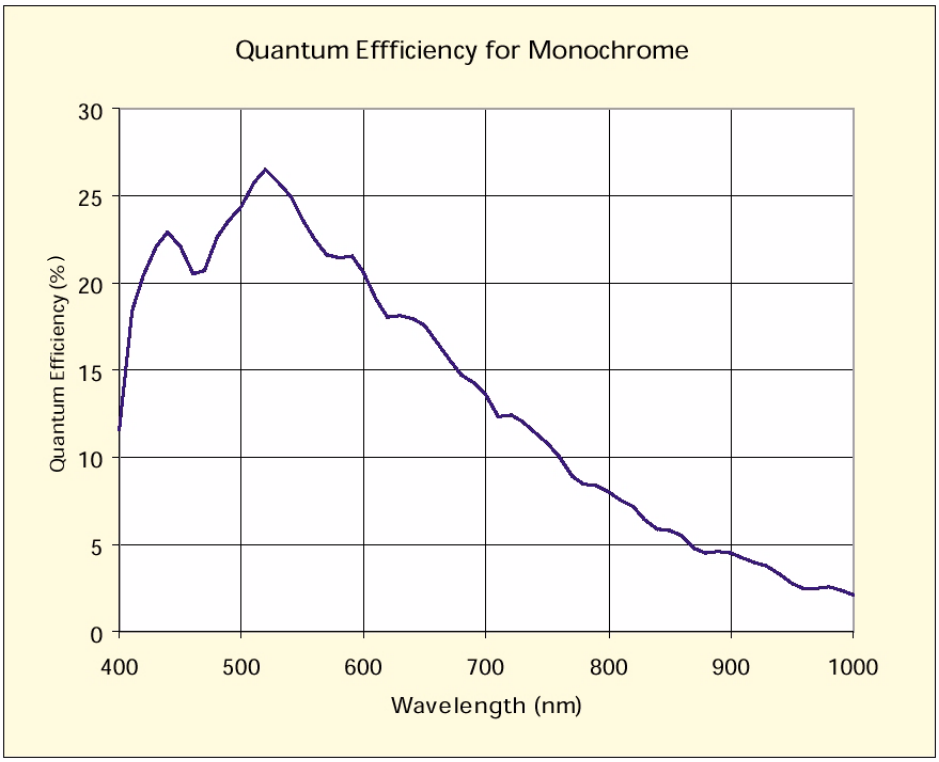


Figure 1-1: Spectral Response for Monochrome **A500k** Cameras

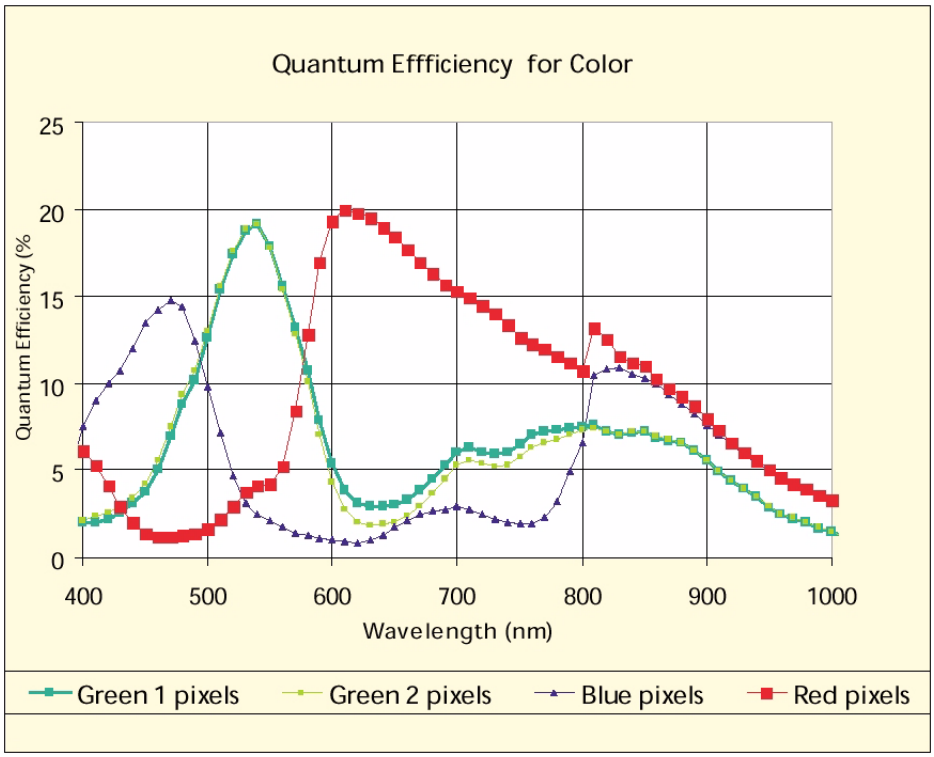


Figure 1-2: Quantum Efficiency for Color **A500kc** Cameras

	Color filter arrays become transparent after 700 nm. To maintain spectral balance, use of a suitable IR cut-off filter is recommended. The filter should transmit in a range of 400 nm to 700 nm. A suitable filter type is the B+W486, for example.

1.4 Environmental Requirements

Temperature and Humidity

Housing temperature during operation:	0° C ... + 50° C (+ 32° F ... + 122° F)
Humidity during operation:	20% ... 80%, relative, non-condensing
Storage temperature:	- 20° C ... + 80° C (- 4° F ... + 176° F)
Storage humidity:	20% ... 80%, relative, non-condensing

You can measure the *inner* temperature via the temperature register. The maximum recommended inner temperature is 60° C (140° F).

Note that the camera components' life time and the image quality are higher the lower the temperature of the camera.

Ventilation

Allow sufficient air circulation around the camera to prevent internal heat build-up in your system and to keep the camera housing temperature during operation below the maximum shown above. Provide additional cooling such as fans or heat sinks if necessary.

1.5 Precautions

Power

Caution!

Making or breaking connections when power is on can result in damage to the camera.

Be sure that all power to your system is switched off before you make or break connections to the camera.

If you can not switch off power, be sure that the power supply connector is the last connector plugged when you make connections to the camera, and the first connector unplugged when you break connections.

Do not remove the camera's serial number label

If the label is removed and the serial number can't be read from the camera's registers, the warranty is void.

Read the manual

Read the manual carefully before using the camera.

Keep foreign matter outside of the camera

Do not open the housing. Touching internal components may damage them.

Be careful not to allow liquids, dust, sand, flammable, or metallic material inside the camera housing. If operated with any foreign matter inside, the camera may fail or cause a fire.

Electromagnetic Fields

Do not operate the camera in the vicinity of strong electromagnetic fields. Avoid electrostatic charging.

Transporting

Only transport the camera in its original packaging. Do not discard the packaging.

Cleaning

Avoid cleaning the surface of the CMOS sensor if possible. If you must clean it, use a soft, lint free cloth dampened with a small quantity of pure alcohol. Do not use methylated alcohol.
Because electrostatic discharge can damage the CMOS sensor, you must use a cloth that will not generate static during cleaning (cotton is a good choice).

To clean the surface of the camera housing, use a soft, dry cloth. To remove severe stains, use a soft cloth dampened with a small quantity of neutral detergent, then wipe dry.

Do not use volatile solvents such as benzine and thinners; they can damage the surface finish.

2 Camera Interface

2.1 Connections

2.1.1 General Description

A500k area scan cameras are interfaced to external circuitry via

- a 26 pin, 0.5“ Mini D Ribbon (MDR) connector to transmit configuration, trigger and image data via Camera Link,
- a microminiature push-pull lock type receptacle to provide power (12 V) to the camera,
- a microminiature push-pull lock type receptacle to provide a signal for an external flash.

A504k/kc and **A503k** area scan cameras have additional connectors:

- a second 26 pin, 0.5“ Mini D Ribbon (MDR) connector to transmit further image data via Camera Link.
- a 15 pin HDSub receptacle for the VGA monitor output (**A504k/kc** only)

The connectors are located on the back of the camera. Figure 2-1 shows the plugs and the status LED which indicates signal integrity and power OK.

Caution!

Making or breaking connections when power is on can result in damage to the camera.

Be sure that all power to your system is switched off before you make or break connections to the camera.

If you can not switch off power, be sure that the power supply connector is the last connector plugged when you make connections to the camera, and the first connector unplugged when you break connections.

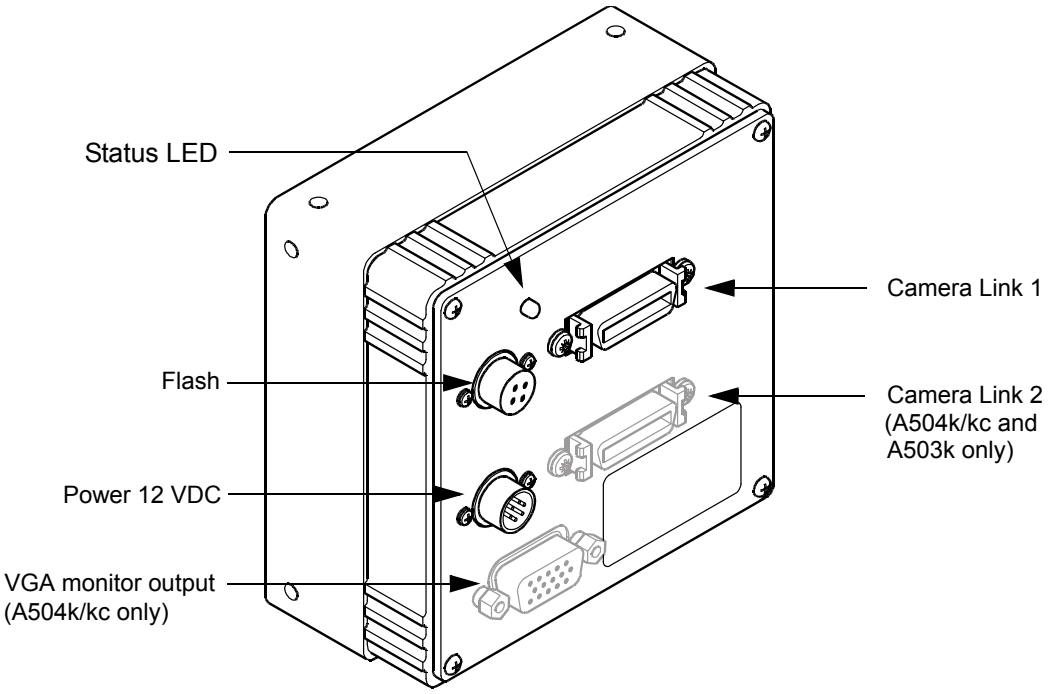


Figure 2-1: **A500k** Connectors and LED

ⓘ	The camera housing is not grounded and is electrically isolated from the circuit boards inside of the camera. Note that the connectors at the camera are described, NOT the connectors required at the connecting cables.

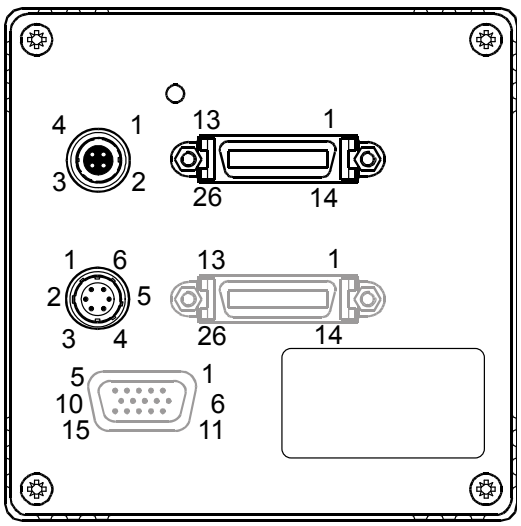


Figure 2-2: **A500k** Pin Numbering

2.1.2 Pin Assignment for the MDR 26 Camera Link Connector(s)

The pin assignment for the MDR 26 pin connector used to interface video data, control signals, and configuration data is given in Table 2-1. Table 2-2 provides the pin assignment for the second MDR 26 pin connector which is only available with the **A504k/kc** and **A503k**.

Camera Link Connector 1:

Pin Number	Signal Name	Direction	Level	Function
1, 13, 14, 26[1]	Gnd	Input	Ground	Ground for the inner shield of the cable
15	X0+	Output	Channel Link LVDS	Data from Channel Link transmitter
2	X0-			
16	X1+	Output	Channel Link LVDS	Data from Channel Link transmitter
3	X1-			
17	X2+	Output	Channel Link LVDS	Data from Channel Link transmitter
4	X2-			
19	X3+	Output	Channel Link LVDS	Data from Channel Link transmitter
6	X3-			
18	XClk+	Output	Channel Link LVDS	Transmit clock from Channel Link transmitter
5	XClk-			
7	SerTC+	Input	RS-644 LVDS	RS-644 Serial communication data receive, channel RxD input
20	SerTC-			
21	SerTFG+	Output	RS-644 LVDS	RS-644 Serial communication data transmit, channel TxD output
8	SerTFG-			
22	CC1+	Input	RS-644 LVDS	ExSync: External trigger
9	CC1-			
10	CC2+	Input	RS-644 LVDS	ExClk. The input is not supported.
23	CC2-			
24	CC3+	Input	RS-644 LVDS	ExFlash: External Flash Trigger
11	CC3-			
12	CC4+	Input	RS-644 LVDS	Not used
25	CC4-			

[1] Pins 1, 13, 14, and 26 are all tied together to GND inside of the camera.

Table 2-1: **A500k** Pin Assignments for the First MDR 26 Pin Connector

Camera Link Connector 2 (**A504k/kc** and **A503k** only):

Pin Number	Signal Name	Direction	Level	Function
1, 13, 14, 26[1]	Gnd	Input	Ground	Ground for the inner shield of the cable
15	Y0+	Output	Channel Link LVDS	Data from Channel Link transmitter
2	Y0-			
16	Y1+	Output	Channel Link LVDS	Data from Channel Link transmitter
3	Y1-			
17	Y2+	Output	Channel Link LVDS	Data from Channel Link transmitter
4	Y2-			
19	Y3+	Output	Channel Link LVDS	Data from Channel Link transmitter
6	Y3-			
18	YClk+	Output	Channel Link LVDS	Transmit clock from Channel Link transmitter
5	YClk-			
7	T+			Connected to T- with 100R; not used
20	T-			Connected to T+ with 100R; not used
21	Z0+	Output	Channel Link LVDS	Data from Channel Link transmitter
8	Z0-			
22	Z1+	Output	Channel Link LVDS	Data from Channel Link transmitter
9	Z1-			
23	Z2+	Output	Channel Link LVDS	Data from Channel Link transmitter
10	Z2-			
25	Z3+	Output	Channel Link LVDS	Data from Channel Link transmitter
12	Z3-			
24	ZClk+	Output	Channel Link LVDS	Transmit clock from Channel Link transmitter
11	ZClk-			

[1] Pins 1, 13, 14, and 26 are all tied together to GND inside of the camera.

Table 2-2: **A504k/kc** and **A503k** Pin Assignments for the Second MDR 26 Pin Connector

2.1.3 Pin Assignment for the Power Connector

The power input connector type is a microminiature push-pull lock type connector, the Hirose HR 10A-7R-6PB. The power supply should deliver 12 V at a minimum of 500 mA (**A504k/kc**), 450 mA (**A503k**) or 250 mA (**A501k/kc**) with a voltage accuracy of ±10%. The pin assignment of the plug is given in Table 2-3.

Pin Number	Signal Name	Direction	Level	Function
1, 2	+12 VDC	Input	12 VDC ± 10%	DC power
3, 4	not connected			
5, 6	DC GND	Input	Ground	DC ground

Table 2-3:**A500k** Pin Assignment for the Power Receptacle

You can use the Hirose HR 10A-7P-6S connector for your cable.

2.1.4 Pin Assignment for the Flash Trigger Receptacle

The Flash trigger output connector type is a microminiature push-pull lock type connector, the Hirose HR 10A-7R-4S. The receptacle provides a signal (FlashOut) for an external flash. This signal can be programmed via the FlashCtrl register. The signal can be deactivated, or tied to an “effective exposure“ signal (Integrate Enabled) generated internally, or tied to the external ExFlash input, or it can be permanently active. The effective exposure is the period when charges are actually accumulated by the sensor.

The output signal can selected to be TTL Active High (default setting), Low Side Switch (Open Collector), or High Side Switch via the Flash Trigger Modes register (see section 4.2.4.16).

The pin assignment is given in Table 2-4. Figure 2-4 shows the three variants of output schematics of the flash trigger connector.

Pin Number	Signal Name	Direction	Level	Function
2	FlashOut	Output	Signal	Flash trigger; the HIGH signal is current limited to 50 mA ±20%.
1, 3	not connected			
4	DC GND	Output	Ground	DC ground

Table 2-4:**A500k** Pin Assignment for the Flash Trigger Receptacle

You can use the Hirose HR 10A-7P-4P connector for your cable.

The FlashOut signal is short-circuit proof. The signal is electrically isolated from other signals in the camera. See the timing diagram in Figure 2-3 and the flash trigger output schematics in Figure 2-4.

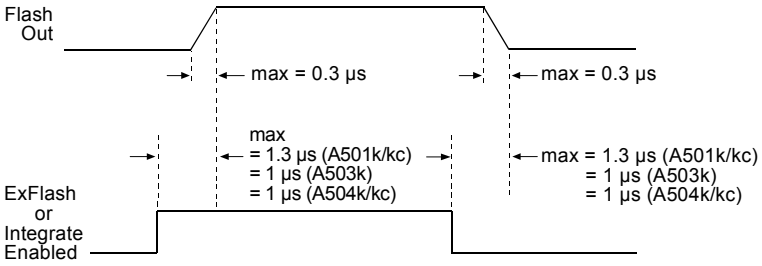


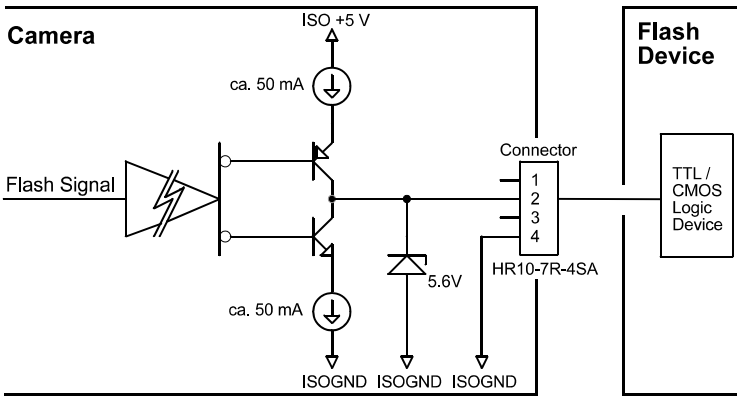
Figure 2-3: FlashOut Signal Timing

TTL Active High (default)

A TTL Active High output signal is typically used together with a TTL / CMOS Logic Device.

The TTL Active High output signal has the following characteristics:

- High output min. 4.5 V at 10 mA output load, shortcut current 50 mA (+40%/- 20%)
- Low output max. 0.5 V at -10 mA output load, shortcut current -50 mA (+40%/- 20%)

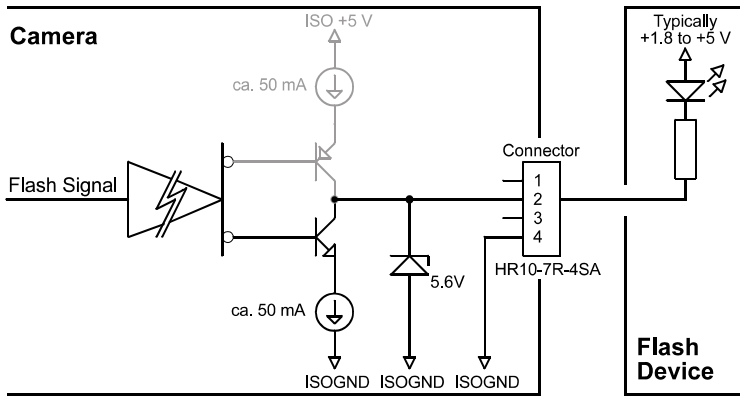


Low Side Switch (Open Collector)

When you select this output signal variant, the upper transistor is deactivated, which is shown by grayed lines in the schematic.

The schematic shows a sample circuit for your flash device.

Select your flash device to ensure that the maximum output current never exceeds 50 mA.



High Side Switch

When you select this output signal variant, the lower transistor is deactivated, which is shown by grayed lines in the schematic.

The schematic shows a sample circuit for your flash device.

Select your flash device to ensure that the maximum output current never exceeds 50 mA.

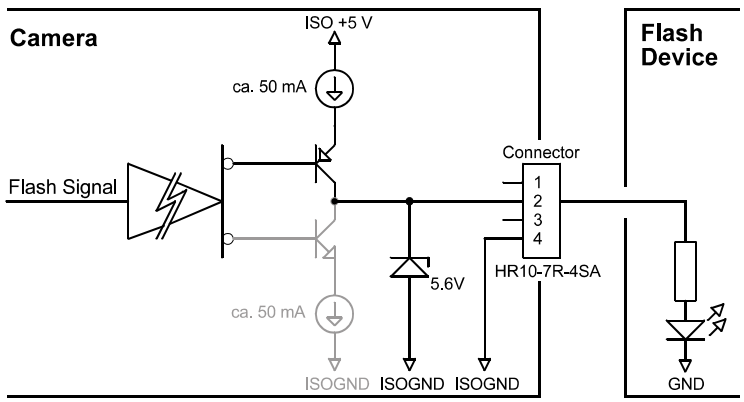


Figure 2-4: Flash Trigger Output Schematics

2.1.5 Pin Assignment for the VGA Monitor Output (A504k/kc Only)

The 15 pin HDSub receptacle for the VGA monitor output transmits 640 x 480 pixels at a rate of 60 fps.

Pin Number	Signal Name	Direction	Function
1	Red Video	Output	Red Video
2	Green Video	Output	Green Video
3	Blue Video	Output	Blue Video
4, 9	not connected		
5, 6, 7, 8, 10, 11	DC GND	Output	DC Ground
12	not connected		SDA is not supported
13	HSync	Output	HSync, 5 V TTL signal
14	VSync	Output	VSync, 5 V TTL signal
15	not connected		SCL is not supported

Table 2-5: **A504k/kc** Pin Assignments for the VGA Monitor Output

2.2 Cable Information

2.2.1 Camera Link Cable

The Camera Link specification requires the use of a standard MDR cable assembly manufactured by 3M™ (part # 14X26-SZLB-XXX-0LC).

The maximum recommended allowed length for the MDR cable used with an **A501k/kc** is 7 meters. The maximum recommended allowed length for the MDR cable used with an **A503k/kc** or **A504k/kc** is 5 meters.

A Camera Link compatible MDR cable assembly is available from Basler as a stock item (part # 1000013905 for a 3 meter cable and part # 1000013906 for a 5 meter cable). Alternatively, you can use the cable assembly manufactured by 3M (part # 14X26-SZLB-XXX-0LC). The **A501k/kc** can also use a base configuration Camera Link cable. See the cable information on the Basler website at: www.baslerweb.com/beitraege/beitrag_en_21085.html.

The maximum cable length will decrease when used in an area with severe ambient electromagnetic interference.

2.2.2 Power Cable

A Hirose, 6-pin locking plug will be shipped with each camera. This plug should be used to terminate the cable on the power supply for the camera. For proper EMI protection, the power supply cable attached to this plug must be a twin-cored, shielded cable. Also, the housing of the Hirose plug must be connected to the cable shield and the cable must be connected to earth ground at the power supply.

2.3 Camera Link Implementation in the A500k

The **A500k** uses a National Semiconductor DS90CR287 as a Channel Link transmitter. For a Channel Link receiver, we recommend that you use the National Semiconductor DS90CR288, the National Semiconductor DS90CR288A or an equivalent. Detailed data sheets for these components are available at the National Semiconductor website (www.national.com). The data sheets contain all of the information that you need to implement Camera Link, including application notes.

	Note that the timing used for sampling the data at the Channel Link receiver in the frame grabber varies from device to device. On some receivers, TTL data must be sampled on the rising edge of the receive clock, and on others, it must be sampled on the falling edge. Also, some devices are available which allow you to select either rising edge or falling edge sampling. For specific timing information, see the data sheet for the receiver that you are using.

The **A500k** uses a National Semiconductor DS90LV048A differential line receiver to receive the RS-644 camera control input signals and the serial communication input signal defined in the Camera Link specification. A DS90LV047A differential line transmitter is used to transmit the serial communication output signal defined in the specification. Detailed spec sheets for these devices are available at the National Semiconductor website (www.national.com).

The **A504k/kc** and the **A503k** use the full configuration of Camera Link with three Channel Link transmitters. The schematic in Figure 2-5 shows the interface for the **A504k/kc.** The schematic in Figure 2-6 shows the interface for the **A503k/kc.**

The **A501k/kc** uses one Channel Link transmitter. The schematic in Figure 2-7 shows the interface for the **A501k/kc** and a typical implementation for the frame grabber interface.

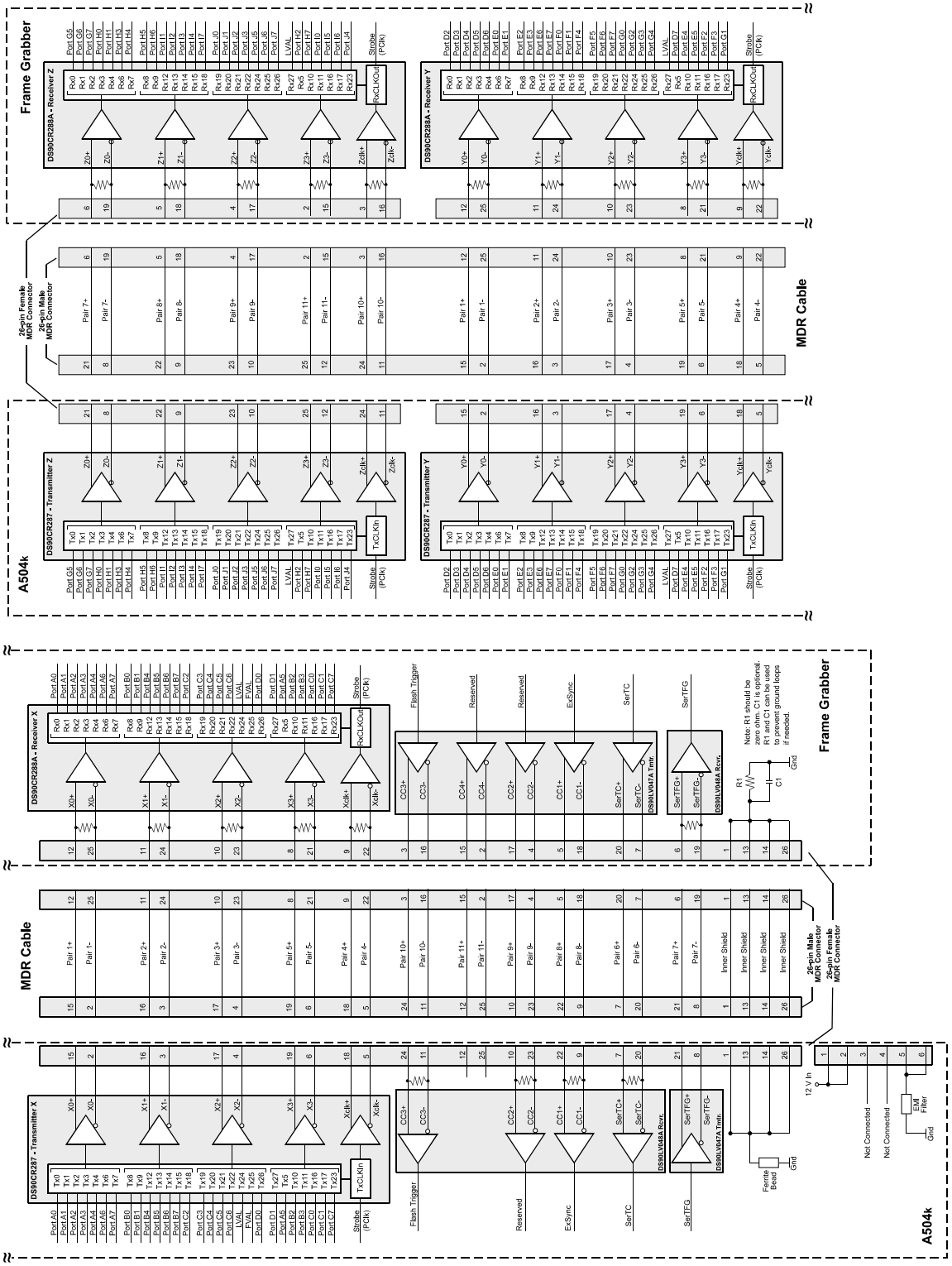


Figure 2-5: **A504k/kc** Camera / Frame Grabber Interface

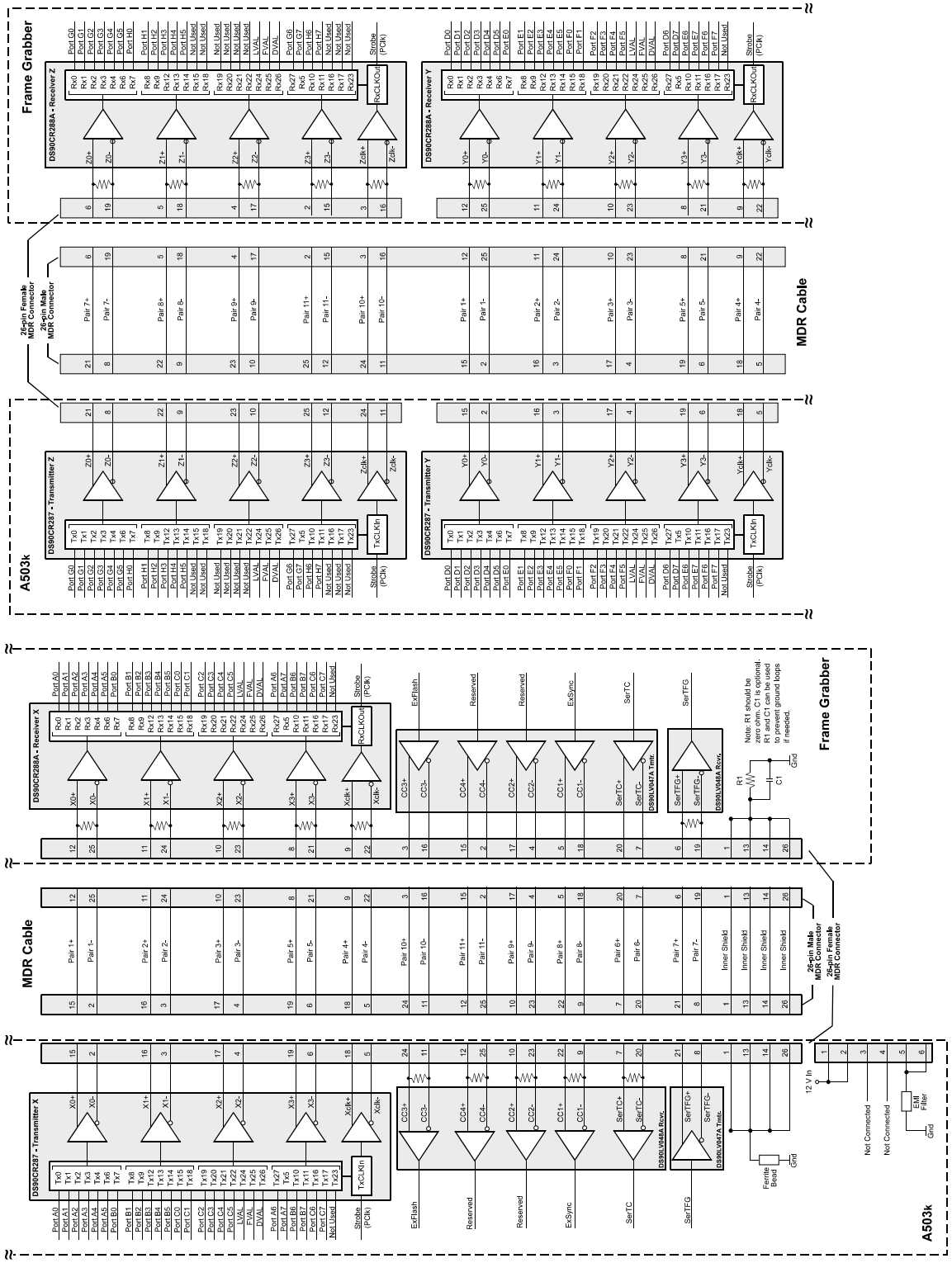


Figure 2-6:**A503k** Camera / Frame Grabber Interface

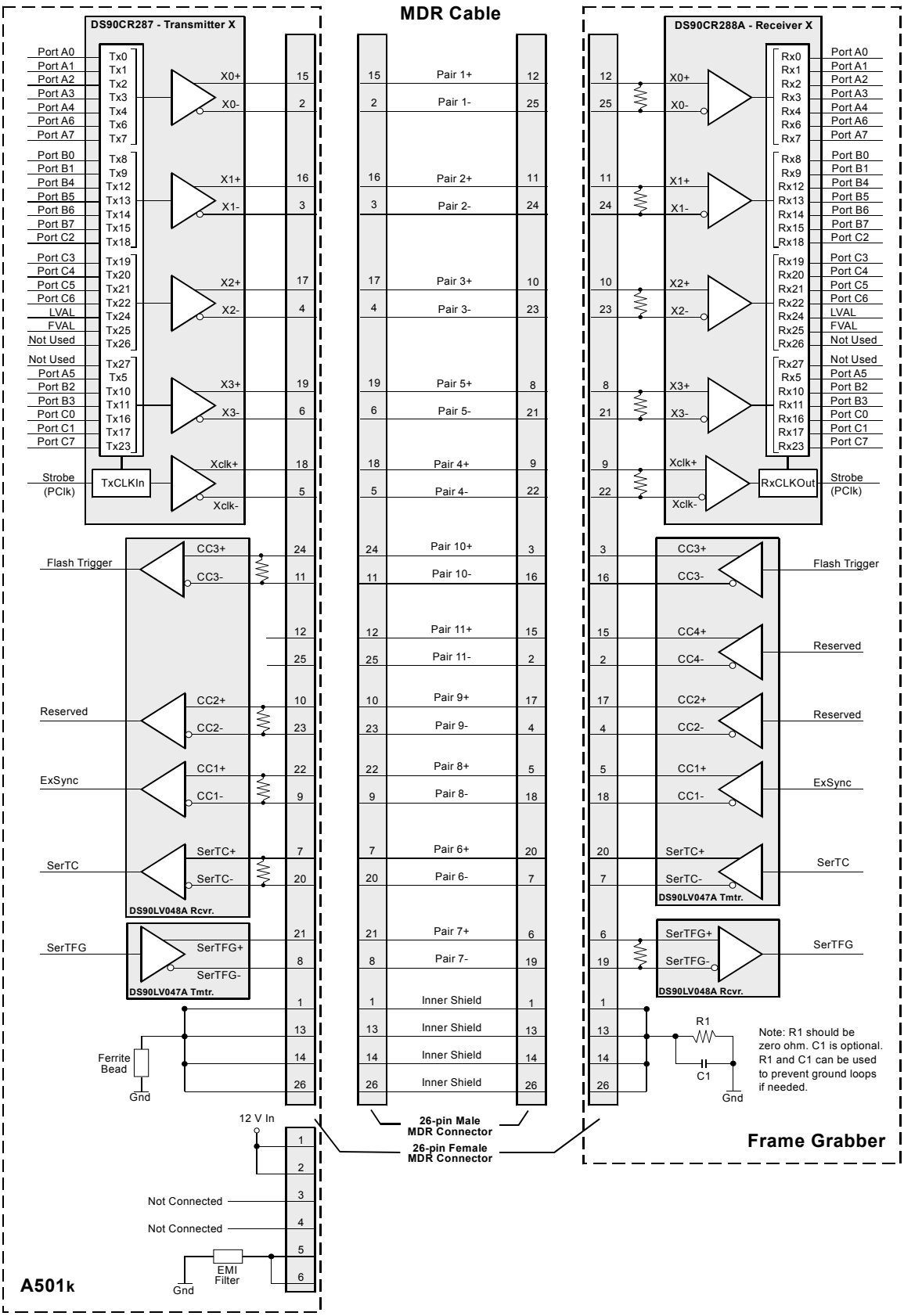


Figure 2-7: **A501k/kc** Camera / Frame Grabber Interface

2.4 Input Signals

The **A500k** receives the RS-644 input signals ExSync, ExClk, ExFlash, and RxD of the serial interface. Section 2.4.1 describes the function of the ExSync signal, section 2.4.2 describes the function of the ExFlash signal. RxD of the serial communication is described in section 2.6.

2.4.1 ExSync: Controls Frame Readout and Exposure Time

The ExSync input signal can be used to control exposure and readout of the **A500k**. ExSync is an LVDS signal as specified for RS-644. The ExSync input corresponds to the camera control signal CC1 as defined in the Camera Link standard. CC2 and CC4 are not used in this camera.

The camera can be programmed to function under the control of an externally generated sync signal (ExSync) in three exposure time control modes. In these modes, edge-controlled, level-controlled and programmable, the ExSync signal is used to control exposure time and frame read out. For more detailed information on the three modes, see section 3.2.

ExSync can be a periodic or non-periodic function. The frequency of the ExSync signal determines the camera's frame rate in these modes.

Note that ExSync is edge sensitive and therefore must toggle. Minimum high time for the ExSync signal is 2 µs, minimum low time 3 µs. These times can change depending on the exposure mode and timing selected (see sections 3.3.2.1 to 3.3.3.4).

2.4.2 ExFlash from the Frame Grabber

The first Channel Link contains an LVDS input for the ExFlash signal. With the corresponding register setting, this input can be tied to the FlashOut signal of the Flash connector. The ExFlash signal is not used by the camera itself. The ExFlash input corresponds to the camera control signal CC3 as defined in the Camera Link standard.

The minimum pulse width of ExFlash is 1 µs. There are no further restrictions.

2.5 Output Signals

Data is output from the **A500k** using the Camera Link standard. The Pixel Clock signal is described in section 2.5.1, the Line Valid signal in section 2.5.2, the Frame Valid signal in section 2.5.3, and the video data in section 2.5.4. How the Video Data is output is described in sections 2.5.5 and 2.5.7. Section 2.5.8 describes the Flash trigger output signal.

The **A504k/kc** uses a modification of the Camera Link standard. The Camera Link standard was modified to be able to transmit 80 bits of data in parallel. Framegrabbers are available for the Basler-specific bit assignment.

2.5.1 Pixel Clock

As shown in Figures 2-5 to 2-7 the pixel clock (PClk, also called strobe) is assigned to the XClk pins (see also Table 2-6, Table 2-7, and Table 2-10). For the **A504k/kc** and **A503k** PClk is also assigned to the YClk and ZClk pins of the Channel Link transmitter (see also Table 2-8 and Table 2-9), as defined in the Camera Link standard.

The pixel clock is used to time the sampling and transmission of pixel data. The Channel Link transmitter(s) used in **A500k** cameras require pixel data to be sampled and transmitted on the rising edge of the clock.

The frequency of the pixel clock is 67.58 MHz for the **A504k/kc** and **A503k** and 50 MHz for the **A501k/kc**. With each Pixel Clock signal, 10 pixels for the **A504k/kc**, 8 pixels for the **A503k**, and 2 pixels for the **A501k/kc** are transmitted.

2.5.2 Line Valid Bit

As shown in Figures 2-8 to 2-13, the line valid bit indicates that a valid line is being transmitted. Pixel data is only valid when this bit is high. 128 (**A504k/kc**), 160 (**A503k**) or 640 (**A501k/kc**) Pixel Clocks are required to transmit one full line. In accord with the camera link standard, line valid is connected to the Channel Link transmitter/receiver pair X, and in the **A504k/kc** and **A503k** also to Y and Z (Figures 2-5 to 2-7, see also Tables 2-6 to 2-10).

2.5.3 Frame Valid Bit

As shown in Figures 2-8 to 2-13, the frame valid bit indicates that a valid frame is being transmitted. One frame can contain 2 to 1024 Line Valid signals. Line valid and pixel data are only valid when the frame valid bit is high. In contrast to the Camera Link standard, frame valid is only connected to Camera Link X in the **A504k/kc** (see Table 2-6).

2.5.4 Video Data

Table 2-6 and Figure 2-5 show the assignment of pixel data bits to the input pins on the Channel Link transmitters X, Y, and Z of the Camera Link in the camera and the corresponding output pins on the Channel Link receivers X, Y, and Z in the frame grabber for the **A504k/kc**. They also show the assignment for the frame valid bit and the line valid bit.These signals and the data transmitted via the three Channel Link transmitter/receiver pairs is not assigned according to the Camera Link standard. The Basler-specific connection is described in Table 2-6. Note that framegrabbers are available for the Basler-specific pin assignment.

Tables 2-7 to 2-9 and Figure 2-6 show the assignment of pixel data bits to the input pins on the Channel Link transmitters X, Y, and Z of the Camera Link in the camera and the corresponding output pins on the Channel Link receivers X, Y, and Z in the frame grabber for the **A503k/kc**. They

also show the assignment for the frame valid bit and the line valid bit.These signals and the data transmitted via the three Channel Link transmitter/receiver pairs are not assigned according to the Camera Link standard. The Basler-specific connection is described in Tables 2-7 to 2-9. Note that framegrabbers are available for the Basler-specific pin assignment.

Table 2-10 and FIgure 2-7 show the assignment of pixel data bits to the input pins on the Channel Link transmitter X of the Camera Link in the camera and the corresponding output pins on the Channel Link receiver X in the frame grabber for the **A501k/kc**. They also show the assignment for the frame valid bit and the line valid bit.

Plug No. 1, Channel Link X				Plug No. 2, Channel Link Y				Plug No. 2, Channel Link Z			
Port	**Camera**	**Frame Grabber**	**Signal**	**Port**	**Camera**	**Frame Grabber**	**Signal**	**Port**	**Camera**	**Frame Grabber**	**Signal**
Port A0	TxIN0	RxOUT0	D0_0	Port D2	TxIN0	RxOUT0	D3_2	Port G5	TxIN0	RxOUT0	D6_5
Port A1	TxIN1	RxOUT1	D0_1	Port D3	TxIN1	RxOUT1	D3_3	Port G6	TxIN1	RxOUT1	D6_6
Port A2	TxIN2	RxOUT2	D0_2	Port D4	TxIN2	RxOUT2	D3_4	Port G7	TxIN2	RxOUT2	D6_7 (MSB)
Port A3	TxIN3	RxOUT3	D0_3	Port D5	TxIN3	RxOUT3	D3_5	Port H0	TxIN3	RxOUT3	D7_0
Port A4	TxIN4	RxOUT4	D0_4	Port D6	TxIN4	RxOUT4	D3_6	Port H1	TxIN4	RxOUT4	D7_1
Port A5	TxIN5	RxOUT5	D0_5	Port D7	TxIN5	RxOUT5	D3_7 (MSB)	Port H2	TxIN5	RxOUT5	D7_2
Port A6	TxIN6	RxOUT6	D0_6	Port E0	TxIN6	RxOUT6	D4_0	Port H3	TxIN6	RxOUT6	D7_3
Port A7	TxIN7	RxOUT7	D0_7 (MSB)	Port E1	TxIN7	RxOUT7	D4_1	Port H4	TxIN7	RxOUT7	D7_4
Port B0	TxIN8	RxOUT8	D1_0	Port E2	TxIN8	RxOUT8	D4_2	Port H5	TxIN8	RxOUT8	D7_5
Port B1	TxIN9	RxOUT9	D1_1	Port E3	TxIN9	RxOUT9	D4_3	Port H6	TxIN9	RxOUT9	D7_6
Port B2	TxIN10	RxOUT10	D1_2	Port E4	TxIN10	RxOUT10	D4_4	Port H7	TxIN10	RxOUT10	D7_7 (MSB)
Port B3	TxIN11	RxOUT11	D1_3	Port E5	TxIN11	RxOUT11	D4_5	Port I0	TxIN11	RxOUT11	D8_0
Port B4	TxIN12	RxOUT12	D1_4	Port E6	TxIN12	RxOUT12	D4_6	Port I1	TxIN12	RxOUT12	D8_1
Port B5	TxIN13	RxOUT13	D1_5	Port E7	TxIN13	RxOUT13	D4_7 (MSB)	Port I2	TxIN13	RxOUT13	D8_2
Port B6	TxIN14	RxOUT14	D1_6	Port F0	TxIN14	RxOUT14	D5_0	PortI 3	TxIN14	RxOUT14	D8_3
Port B7	TxIN15	RxOUT15	D1_7 (MSB)	Port F1	TxIN15	RxOUT15	D5_1	Port I4	TxIN15	RxOUT15	D8_4
Port C0	TxIN16	RxOUT16	D2_0	Port F2	TxIN16	RxOUT16	D5_2	Port I5	TxIN16	RxOUT16	D8_5
Port C1	TxIN17	RxOUT17	D2_1	Port F3	TxIN17	RxOUT17	D5_3	Port I6	TxIN17	RxOUT17	D8_6
Port C2	TxIN18	RxOUT18	D2_2	Port F4	TxIN18	RxOUT18	D5_4	Port I7	TxIN18	RxOUT18	D8_7 (MSB)
Port C3	TxIN19	RxOUT19	D2_3	Port F5	TxIN19	RxOUT19	D5_5	Port J0	TxIN19	RxOUT19	D9_0
Port C4	TxIN20	RxOUT20	D2_4	Port F6	TxIN20	RxOUT20	D5_6	Port J1	TxIN20	RxOUT20	D9_1
Port C5	TxIN21	RxOUT21	D2_5	Port F7	TxIN21	RxOUT21	D5_7 (MSB)	Port J2	TxIN21	RxOUT21	D9_2
Port C6	TxIN22	RxOUT22	D2_6	Port G0	TxIN22	RxOUT22	D6_0	Port J3	TxIN22	RxOUT22	D9_3
Port C7	TxIN23	RxOUT23	D2_7 (MSB)	Port G1	TxIN23	RxOUT23	D6_1	Port J4	TxIN23	RxOUT23	D9_4
LVAL	TxIN24	RxOUT24	Line Valid	Port G2	TxIN24	RxOUT24	D6_2	Port J5	TxIN24	RxOUT24	D9_5
FVAL	TxIN25	RxOUT25	Frame Valid	Port G3	TxIN25	RxOUT25	D6_3	Port J6	TxIN25	RxOUT25	D9_6
Port D0	TxIN26	RxOUT26	D3_0	Port G4	TxIN26	RxOUT26	D6_4	Port J7	TxIN26	RxOUT26	D9_7 (MSB)
Port D1	TxIN27	RxOUT27	D3_1	LVAL	TxIN27	RxOUT27	Line Valid	LVAL	TxIN27	RxOUT27	Line Valid
PClk	TxCLKIn	RxCLKOut	Pixel Clock A, B, C	PClk	TxCLKIn	RxCLKOut	Pixel Clock D, E, F	PClk	TxCLKIn	RxCLKOut	Pixel Clock G, H, i, J

Table 2-6: Bit Assignments of the Three Channel Link Transmitters (**A504k/kc**)

Note that the bit assignment of the **A504k/kc** does NOT follow the current Camera Link standard in every respect:

- Channel Link transmitters Y and Z do not transmit an FVAL signal.
- The data lines are assigned to different input pins.
- The data lines are also assigned to the spare pins and the pins normally assigned to FVAL and DVAL.

Note that framegrabbers are available for the Basler-specific bit assignment.

Plug No. 1, Transmitter X			
Port	**Camera**	**Frame Grabber**	**Signal**
Port A0	TxIN0	RxOUT0	D0 Bit 0
Port A1	TxIN1	RxOUT1	D0 Bit 1
Port A2	TxIN2	RxOUT2	D0 Bit 2
Port A3	TxIN3	RxOUT3	D0 Bit 3
Port A4	TxIN4	RxOUT4	D0 Bit 4
Port A5	TxIN6	RxOUT6	D0 Bit 5
Port A6	TxIN27	RxOUT27	D0 Bit 6
Port A7	TxIN5	RxOUT5	D0 Bit 7 (MSB)
Port B0	TxIN7	RxOUT7	D1 Bit 0
Port B1	TxIN8	RxOUT8	D1 Bit 1
Port B2	TxIN9	RxOUT9	D1 Bit 2
Port B3	TxIN12	RxOUT12	D1 Bit 3
Port B4	TxIN13	RxOUT13	D1 Bit 4
Port B5	TxIN14	RxOUT14	D1 Bit 5
Port B6	TxIN10	RxOUT10	D1 Bit 6
Port B7	TxIN11	RxOUT11	D1 Bit 7 (MSB)
Port C0	TxIN15	RxOUT15	D2 Bit 0
Port C1	TxIN18	RxOUT18	D2 Bit 1
Port C2	TxIN19	RxOUT19	D2 Bit 2
Port C3	TxIN20	RxOUT20	D2 Bit 3
Port C4	TxIN21	RxOUT21	D2 Bit 4
Port C5	TxIN22	RxOUT22	D2 Bit 5
Port C6	TxIN16	RxOUT16	D2 Bit 6
Port C7	TxIN17	RxOUT17	D2 Bit 7 (MSB)
LVAL	TxIN24	RxOUT24	Line Valid
FVAL	TxIN25	RxOUT25	Frame Valid
DVAL	TxIN26	RxOUT26	Line Valid
Not Used	TxIN23	RxOUT23	Not Used
PClk	TxCLKIn	RxCLKOut	Pixel Clock

Table 2-7: Bit Assignments of the Channel Link Transmitter X for the **A503k** (Plug 1)

Plug No. 2, Transmitter Y			
Port	**Camera**	**Frame Grabber**	**Signal**
Port D0	TxIN0	RxOUT0	D3 Bit 0
Port D1	TxIN1	RxOUT1	D3 Bit 1
Port D2	TxIN2	RxOUT2	D3 Bit 2
Port D3	TxIN3	RxOUT3	D3 Bit 3
Port D4	TxIN4	RxOUT4	D3 Bit 4
Port D5	TxIN6	RxOUT6	D3 Bit 5
Port D6	TxIN27	RxOUT27	D3 Bit 6
Port D7	TxIN5	RxOUT5	D3 Bit 7 (MSB)
Port E0	TxIN7	RxOUT7	D4 Bit 0
Port E1	TxIN8	RxOUT8	D4 Bit 1
Port E2	TxIN9	RxOUT9	D4 Bit 2
Port E3	TxIN12	RxOUT12	D4 Bit 3
Port E4	TxIN13	RxOUT13	D4 Bit 4
Port E5	TxIN14	RxOUT14	D4 Bit 5
Port E6	TxIN10	RxOUT10	D4 Bit 6
Port E7	TxIN11	RxOUT11	D4 Bit 7 (MSB)
Port F0	TxIN15	RxOUT15	D5 Bit 0
Port F1	TxIN18	RxOUT18	D5 Bit 1
Port F2	TxIN19	RxOUT19	D5 Bit 2
Port F3	TxIN20	RxOUT20	D5 Bit 3
Port F4	TxIN21	RxOUT21	D5 Bit 4
Port F5	TxIN22	RxOUT22	D5 Bit 5
Port F6	TxIN16	RxOUT16	D5 Bit 6
Port F7	TxIN17	RxOUT17	D5 Bit 7 (MSB)
LVAL	TxIN24	RxOUT24	Line Valid
FVAL	TxIN25	RxOUT25	Frame Valid
DVAL	TxIN26	RxOUT26	Line Valid
Not Used	TxIN23	RxOUT23	Not Used
PClk	TxCLKIn	RxCLKOut	Pixel Clock

Table 2-8: Bit Assignments of the Channel Link Transmitter Y for the **A503k** (Plug 2)

Plug No. 2, Transmitter Z			
Port	**Camera**	**Frame Grabber**	**Signal**
Port G0	TxIN0	RxOUT0	D6 Bit 0
Port G1	TxIN1	RxOUT1	D6 Bit 1
Port G2	TxIN2	RxOUT2	D6 Bit 2
Port G3	TxIN3	RxOUT3	D6 Bit 3
Port G4	TxIN4	RxOUT4	D6 Bit 4
Port G5	TxIN6	RxOUT6	D6 Bit 5
Port G6	TxIN27	RxOUT27	D6 Bit 6
Port G7	TxIN5	RxOUT5	D6 Bit 7 (MSB)
Port H0	TxIN7	RxOUT7	D7 Bit 0
Port H1	TxIN8	RxOUT8	D7 Bit 1
Port H2	TxIN9	RxOUT9	D7 Bit 2
Port H3	TxIN12	RxOUT12	D7 Bit 3
Port H4	TxIN13	RxOUT13	D7 Bit 4
Port H5	TxIN14	RxOUT14	D7 Bit 5
Port H6	TxIN10	RxOUT10	D7 Bit 6
Port H7	TxIN11	RxOUT11	D7 Bit 7 (MSB)
Not Used	TxIN15	RxOUT15	Not Used
Not Used	TxIN18	RxOUT18	Not Used
Not Used	TxIN19	RxOUT19	Not Used
Not Used	TxIN20	RxOUT20	Not Used
Not Used	TxIN21	RxOUT21	Not Used
Not Used	TxIN22	RxOUT22	Not Used
Not Used	TxIN16	RxOUT16	Not Used
Not Used	TxIN17	RxOUT17	Not Used
LVAL	TxIN24	RxOUT24	Line Valid
FVAL	TxIN25	RxOUT25	Frame Valid
DVAL	TxIN26	RxOUT26	Line Valid
Not Used	TxIN23	RxOUT23	Not Used
PClk	TxCLKIn	RxCLKOut	Pixel Clock

Table 2-9: Bit Assignments of the Channel Link Transmitter Z for the **A503k** (Plug 2)

Port	Camera	Frame Grabber	Signal
Port A0	TxIN0	RxOUT0	D0 Bit 0
Port A1	TxIN1	RxOUT1	D0 Bit 1
Port A2	TxIN2	RxOUT2	D0 Bit 2
Port A3	TxIN3	RxOUT3	D0 Bit 3
Port A4	TxIN4	RxOUT4	D0 Bit 4
Port A5	TxIN5	RxOUT5	D0 Bit 5
Port A6	TxIN6	RxOUT6	D0 Bit 6
Port A7	TxIN7	RxOUT7	D0 Bit 7 (MSB)
Port B0	TxIN8	RxOUT8	D1 Bit 0
Port B1	TxIN9	RxOUT9	D1 Bit 1
Port B2	TxIN10	RxOUT10	D1 Bit 2
Port B3	TxIN11	RxOUT11	D1 Bit 3
Port B4	TxIN12	RxOUT12	D1 Bit 4
Port B5	TxIN13	RxOUT13	D1 Bit 5
Port B6	TxIN14	RxOUT14	D1 Bit 6
Port B7	TxIN15	RxOUT15	D1 Bit 7 (MSB)
Port C0	TxIN16	RxOUT16	Not Used
Port C1	TxIN17	RxOUT17	Not Used
Port C2	TxIN18	RxOUT18	Not Used
Port C3	TxIN19	RxOUT19	Not Used
Port C4	TxIN20	RxOUT20	Not Used
Port C5	TxIN21	RxOUT21	Not Used
Port C6	TxIN22	RxOUT22	Not Used
Port C7	TxIN23	RxOUT23	Not Used
LVAL	TxIN24	RxOUT24	Line Valid
FVAL	TxIN25	RxOUT25	Frame Valid
Not Used	TxIN26	RxOUT26	Not Used
Not Used	TxIN27	RxOUT27	Not Used
PClk	TxCLKIn	RxCLKOut	Pixel Clock

Table 2-10: Bit Assignments of the Channel Link Transmitter for the **A501k/kc**

2.5.5 Video Data Output for the A504k/kc

A504k cameras output the video data in a 10 x 8 Bit data stream.

The pixel clock is used to time data sampling and transmission. As shown in Figures 2-8 and 2-9, the camera samples and transmits data on each rising edge of the pixel clock.

The image has a maximum size of 1280 x 1024 pixels that are transmitted with a Pixel Clock frequency of 67.58 MHz over the three Channel Link transmitter/receiver pairs X, Y and Z. With each clock cycle ten pixels at a depth of 8 Bits are transmitted in parallel. Therefore one line takes a maximum of 128 clock cycles to become transmitted. For more details about sensor timing, refer to the Micron MV13 data sheet (www.micron.com).

Due to the internal sensor design, the starting columns of areas of interest (AOIs; see section 3.11) are restricted to values of multiples of 10 + 1. AOI widths, expressed in columns, are restricted to multiples of 10. For details read the register description of the AOI Starting Column and the AOI Width register. Image is transmitted line by line from top left to bottom right. Frame Valid (FVAL) and Line Valid (LVAL) mark the beginning and duration of frame and line.

The line valid bit indicates that a valid line is being transmitted. Pixel data is valid when the line valid bit is high.

The sensor outputs 10 Bits, but two bits output from each ADC are dropped and only 8 bits of data per pixel is transmitted. The digital shift function selects the bits to be dropped (see section 3.10).

The data sequence outlined below, along with Figures 2-8 and 2-9, describe what is happening at the inputs to the Channel Link transmitters in the camera.

Note that the timing used for sampling the data at the Channel Link receivers in the frame grabber varies from device to device. On some receivers, data must be sampled on the rising edge of the pixel clock (receive clock), and on others, it must be sampled on the falling edge. Also, some devices are available which allow you to select either rising edge or falling edge sampling. For specific timing information, see the data sheet for the receiver that you are using .

Video Data Sequence for the A504k/kc

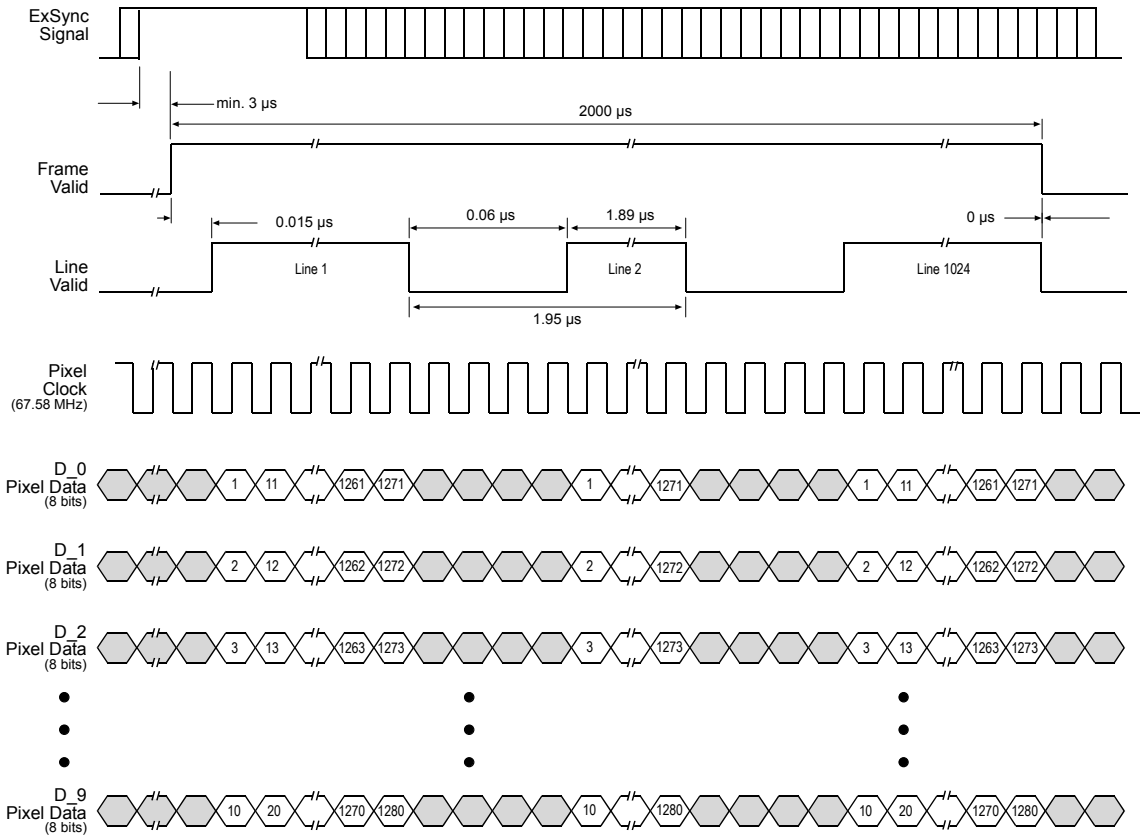
When the camera is not transmitting valid data, the frame valid and line valid bits sent on each cycle of the pixel clock will be low. The camera can acquire a frame and, at the same time, send the previous frame. It can also first acquire a frame and then send it. When Frame valid becomes high, the camera starts to send valid data:

- On the pixel clock cycle where frame data transmission begins, the frame valid bit will become high. One pixel clock later, the line valid bit will become high (if AOI Starting Column = 0).
- On the pixel clock cycle where data transmission for line one begins, the line valid bit will become high. Ten data streams are transmitted in parallel during this clock cycle. The first pixel is the first pixel in the first data stream D_0. The second pixel is the first pixel in the second data stream D_1, and so on. The tenth data stream D_10 contains the tenth pixel. 8 bits will contain the data for each pixel.
- On the next cycle of the pixel clock, the line valid bit will be high. The eleventh pixel is the second pixel in the D_0 data stream. The twelfth pixel is the second pixel in the D_1 data stream, and so on. The tenth D_9 data stream contains the twentieth pixel. 8 bits will contain the data for each pixel.
- On the next cycle of the pixel clock, the line valid bit will be high. The twenty first pixel is the third pixel in the D_0 data stream. The twenty second pixel is the third pixel in the D_1 data

stream, and so on. The tenth D_9 data stream contains the thirtieth pixel. 8 bits will contain the data for each pixel.

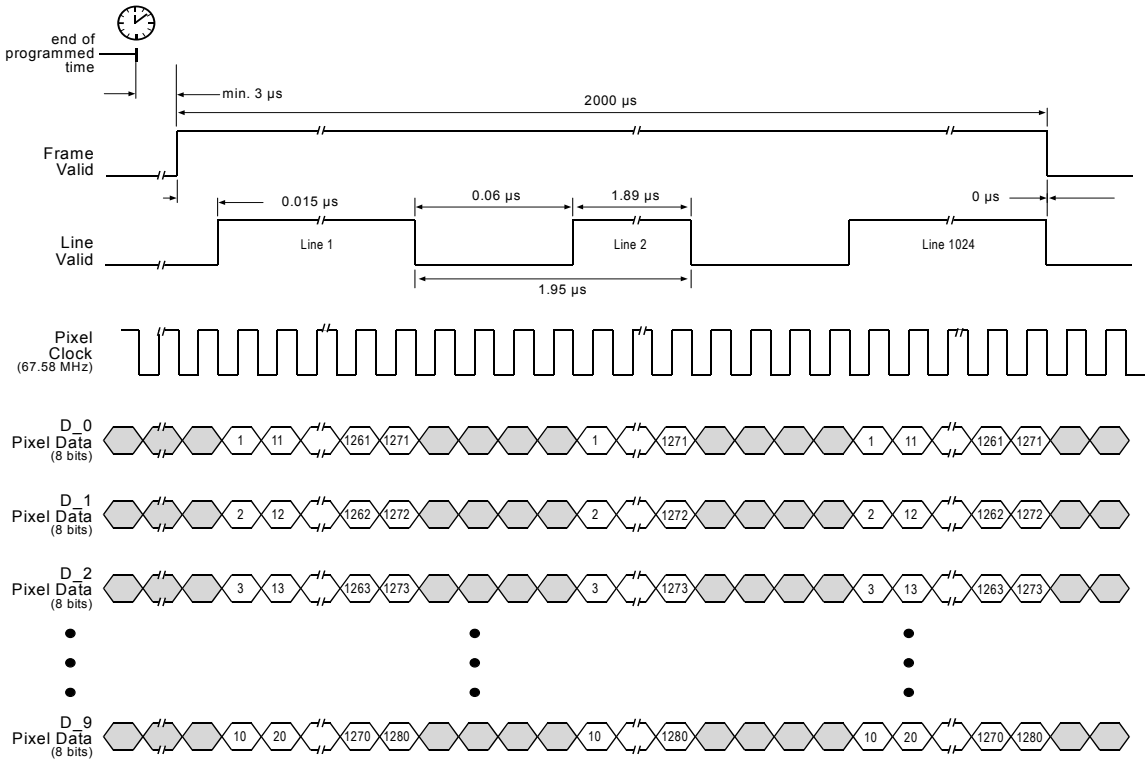
- This pattern will continue until all of the pixel data for each data stream for line one has been transmitted. (A total of 128 cycles for the **A504k/kc**)
- Line valid becomes low for four pixel clocks.
- On the pixel clock cycle where data transmission for line two begins, the line valid bit will become high. Ten data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the first, second, third ... tenth pixel of line number two.
- On the next cycle of the pixel clock, the line valid bit will be high. Ten data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the eleventh, twelfth, thirteenth ... twentieth pixel of line number two.
- On the next cycle of the pixel clock, the line valid bit will be high. Ten data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the twenty first, twenty second, twenty third ... thirtieth pixel of line number two.
- This pattern will continue until all of the pixel data for each data stream for line two has been transmitted. (A total of 128 cycles.)
- After all of the pixels in line two have been transmitted, the line valid bit will become low for four cycles indicating that valid data for line two is no longer being transmitted.
- The camera will continue to transmit pixel data for each line as described above until all of the lines in the frame have been transmitted. After all of the lines have been transmitted, the frame valid bit will become low at the same time as line valid indicating that a valid frame is no longer being transmitted.
- Frame valid will remain low for at least 3 pixel clock cycles until the next frame starts.

Figure 2-8 shows the data sequence when the camera is operating in edge-controlled or level-controlled exposure mode and Figure 2-9 shows the data sequence when the camera is operating in programmable exposure mode.



This diagram assumes that the area of interest feature is not being used. With the area of interest feature enabled, the number of pixels transferred could be smaller.

Figure 2-8: 8 Bit Output Mode with Edge or Level-controlled Exposure for the A504k/kc



This diagram assumes that the area of interest feature is not being used. With the area of interest feature enabled, the number of pixels transferred could be smaller.

Figure 2-9: 8 Bit Output Mode with Programmable Exposure for ths A504k/kc

2.5.6 Video Data Output for the A503k

A503k cameras output the video data in an 8 x 8 Bit data stream.

The pixel clock is used to time data sampling and transmission. As shown in Figures 2-10 and 2-11, the camera samples and transmits data on each rising edge of the pixel clock.

The image has a maximum size of 1280 x 1024 pixels that are transmitted with a Pixel Clock frequency of 67.58 MHz over the three Channel Link transmitter/receiver pairs X, Y and Z. With each clock cycle, eight pixels at a depth of 8 Bits are transmitted in parallel. Therefore one line takes a maximum of 160 clock cycles to become transmitted. For more details about sensor timing, refer to the Micron MV13 data sheet (www.micron.com).

Due to the internal sensor design, the starting columns of areas of interest (AOIs; see section 3.11) are restricted to values of multiples of 10 + 1. AOI widths, expressed in columns, are restricted to multiples of 40. For details, read the register description of the AOI Starting Column and the AOI Width register. The image is transmitted line by line from top left to bottom right. Frame Valid (FVAL) and Line Valid (LVAL) mark the beginning and duration of frame and line.

The line valid bit indicates that a valid line is being transmitted. Pixel data is valid when the line valid bit is high.

The sensor outputs 10 Bits, but two bits output from each ADC are dropped and only 8 bits of data per pixel is transmitted. The digital shift function selects the bits to be dropped (see section 3.10).

The data sequence outlined below, along with Figures 2-10 and 2-11, describe what is happening at the inputs to the Channel Link transmitters in the camera.

Note that the timing used for sampling the data at the Channel Link receivers in the frame grabber varies from device to device. On some receivers, data must be sampled on the rising edge of the pixel clock (receive clock), and on others, it must be sampled on the falling edge. Also, some devices are available which allow you to select either rising edge or falling edge sampling. For specific timing information, see the data sheet for the receiver that you are using .

Video Data Sequence for the A503k

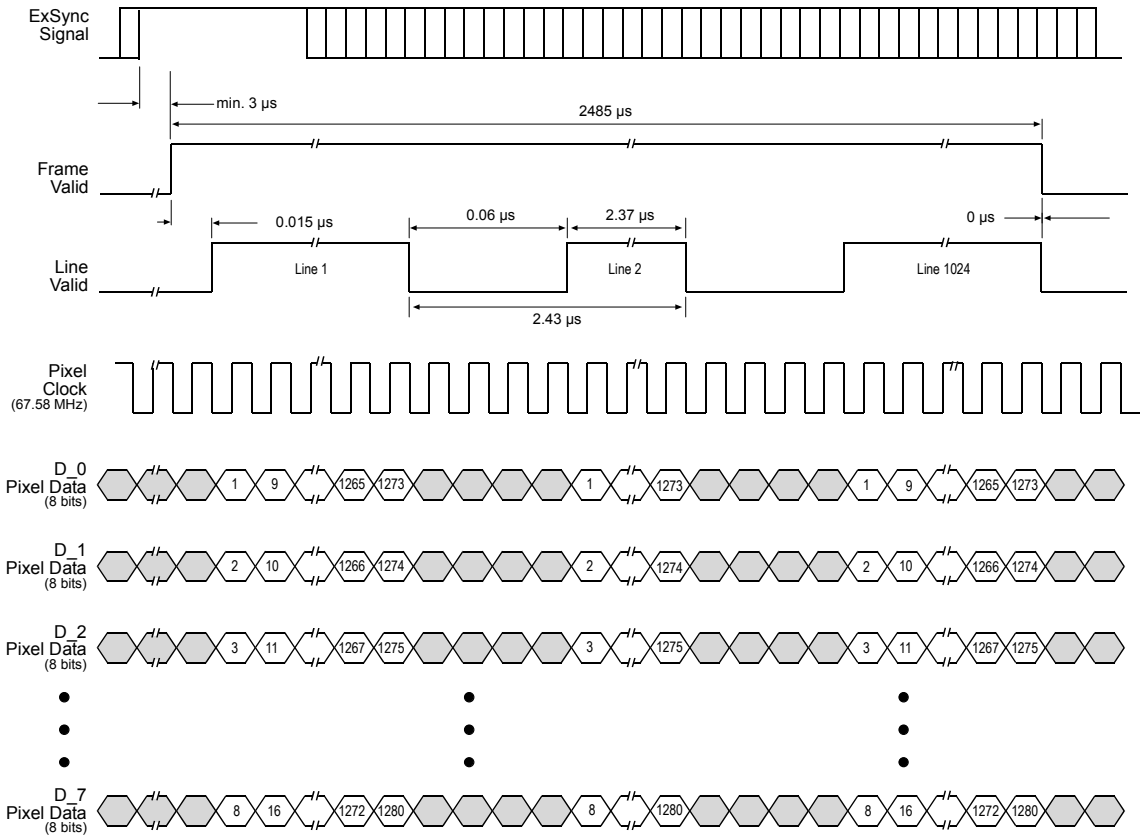
When the camera is not transmitting valid data, the frame valid and line valid bits sent on each cycle of the pixel clock will be low. The camera can acquire a frame and, at the same time, send the previous frame. It can also first acquire a frame and then send it. When Frame valid becomes high, the camera starts to send valid data:

- On the pixel clock cycle where frame data transmission begins, the frame valid bit will become high. One pixel clock later, the line valid bit will become high (if AOI Starting Column = 0).
- On the pixel clock cycle where data transmission for line one begins, the line valid bit will become high. Eight data streams are transmitted in parallel during this clock cycle. The first pixel is the first pixel in the first data stream D_0. The second pixel is the first pixel in the data stream D_1, and so on. The eighth pixel is the first pixel in the data stream D_7. The data for each pixel will be at eight bit depth.
- On the next cycle of the pixel clock, the line valid bit will be high. The ninth pixel is the second pixel in the D_0 data stream. The tenth pixel is the second pixel in the D_1 data stream, and so on. The sixteenth pixel is is the second pixel in the D_7 data stream. The data for each pixel will be at eight bit depth.
- On the next cycle of the pixel clock, the line valid bit will be high. The seventeenth pixel is the third pixel in the D_0 data stream. The eighteenth pixel is the third pixel in the D_1 data

stream, and so on. The twentyfourth pixel is the third pixel in the D_7 data stream. The data for each pixel will be at eight bit depth.

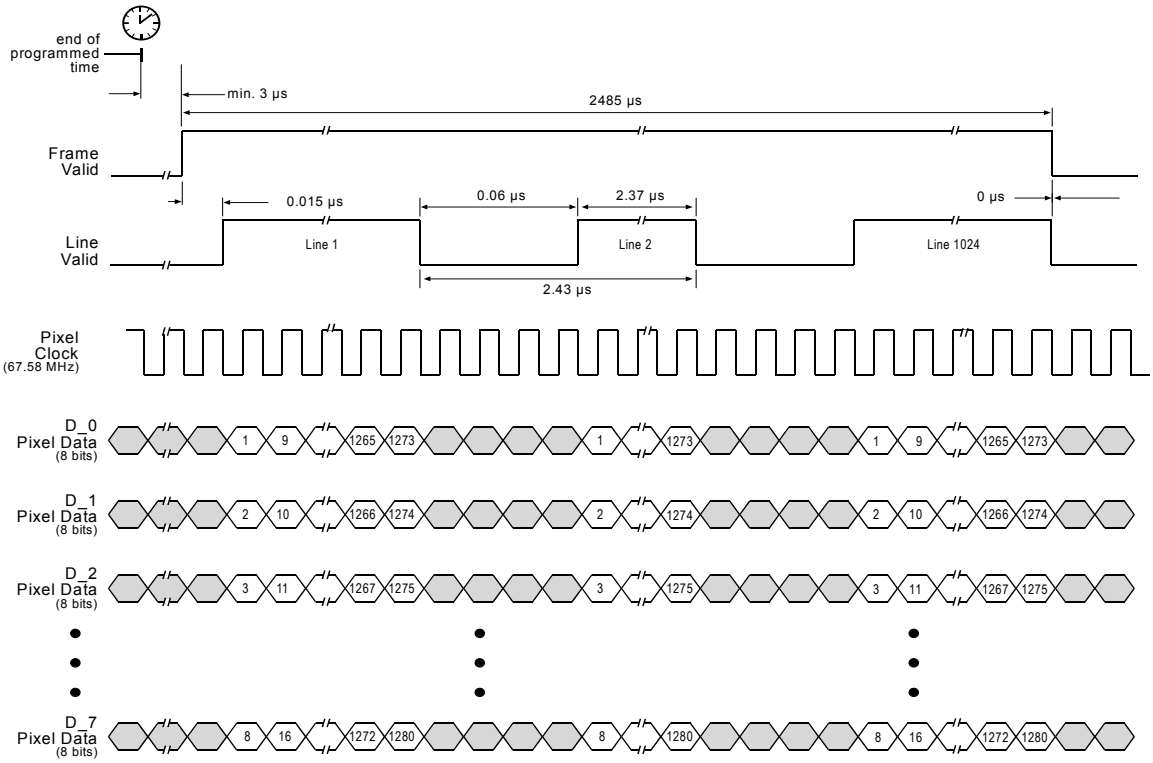
- This pattern will continue until all of the pixel data for each data stream for line one has been transmitted. (A total of 160 cycles for the **A503k**).
- Line valid becomes low for four pixel clocks.
- On the pixel clock cycle where data transmission for line two begins, the line valid bit will become high. Eight data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the first, second, third ... eighth pixel of line number two.
- On the next cycle of the pixel clock, the line valid bit will be high. Eight data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the ninth, tenth, eleventh ... sixteenth pixel of line number two.
- On the next cycle of the pixel clock, the line valid bit will be high. Eight data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the seventeenth, einghteenth, nineteenth ... twenty fourth pixel of line number two.
- This pattern will continue until all of the pixel data for each data stream for line two has been transmitted. (A total of 160 cycles.)
- After all of the pixels in line two have been transmitted, the line valid bit will become low for four cycles indicating that valid data for line two is no longer being transmitted.
- The camera will continue to transmit pixel data for each line as described above until all of the lines in the frame have been transmitted. After all of the lines have been transmitted, the frame valid bit will become low at the same time as line valid indicating that a valid frame is no longer being transmitted.
- Frame valid will remain low for at least 3 pixel clock cycles until the next frame starts.

Figure 2-10 shows the data sequence when the camera is operating in edge-controlled or level-controlled exposure mode and Figure 2-11 shows the data sequence when the camera is operating in programmable exposure mode.



This diagram assumes that the area of interest feature is not being used. With the area of interest feature enabled, the number of pixels transferred could be smaller.

Figure 2-10: 8 Bit Output Mode with Edge or Level-controlled Exposure for the A503k



This diagram assumes that the area of interest feature is not being used. With the area of interest feature enabled, the number of pixels transferred could be smaller.

Figure 2-11: 8 Bit Output Mode with Programmable Exposure for the A503k

2.5.7 Video Data Output for the A501k/kc

A501k/kc cameras output the video data in a 2 x 8 Bit data stream.

The pixel clock is used to time data sampling and transmission. As shown in Figures 2-12 and 2-13, the camera samples and transmits data on each rising edge of the pixel clock.

The image has a maximum size of 1280 x 1024 pixels that are transmitted with a Pixel Clock frequency of 50 MHz over the Channel Link transmitter/receiver pair X. With each clock cycle two pixels at a depth of 8 Bits are transmitted in parallel. Therefore one line takes a maximum of 640 clock cycles to become transmitted. For more details about sensor timing, refer to the Micron MV13 data sheet (www.micron.com).

Due to the internal sensor design, the starting columns of areas of interest (AOIs; see section 3.11) are restricted to values of multiples of 10 + 1. AOI widths, expressed in columns, are restricted to multiples of 10. For details, read the register description of the AOI Starting Column and the AOI Width register. Image is transmitted line by line from top left to bottom right. Frame Valid (FVAL) and Line Valid (LVAL) mark the beginning and duration of frame and line.

The line valid bit indicates that a valid line is being transmitted. Pixel data is valid when the line valid bit is high.

The sensor outputs 10 Bits, but the two bits output from each ADC are dropped and only 8 bits of data per pixel is transmitted. The digital shift function selects the bits to be dropped (see section 3.10).

The data sequence outlined below, along with Figures 2-12 and 2-13, describe what is happening at the inputs to the Channel Link transmitters in the camera.

Note that the timing used for sampling the data at the Channel Link receivers in the frame grabber varies from device to device. On some receivers, data must be sampled on the rising edge of the pixel clock (receive clock), and on others, it must be sampled on the falling edge. Also, some devices are available which allow you to select either rising edge or falling edge sampling. For specific timing information, see the data sheet for the receiver that you are using .

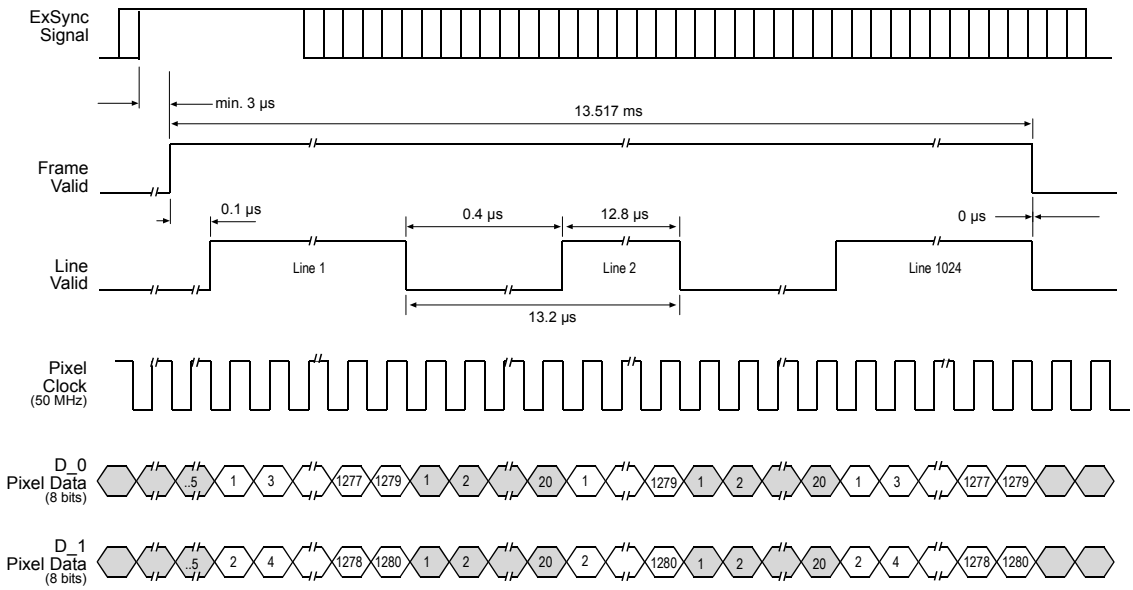
Video Data Sequence for the A501k/kc

When the camera is not transmitting valid data, the frame valid and line valid bits sent on each cycle of the pixel clock will be low. The camera can acquire a frame and, at the same time, send the previous frame. It can also first acquire a frame and then send it. When Frame valid becomes high, the camera starts to send valid data:

- On the pixel clock cycle where frame data transmission begins, the frame valid bit will become high. Five pixel clocks later, the line valid bit will become high (if AOI Starting Column = 0).
- On the pixel clock cycle where data transmission for line one begins, the line valid bit will become high. Two data streams are transmitted in parallel during this clock cycle. The first pixel is the first pixel in the first data stream D_0. The second pixel is the first pixel in the second data stream D_1. 8 bits will contain the data for each pixel.
- On the next cycle of the pixel clock, the line valid bit will be high. The third pixel is the second pixel in the D_0 data stream. The fourth pixel is the second pixel in the D_1 data stream. 8 bits will contain the data for each pixel.
- On the next cycle of the pixel clock, the line valid bit will be high. The fifth pixel is the third pixel in the D_0 data stream. The sixth pixel is the third pixel in the D_1 data stream. 8 bits will contain the data for each pixel.

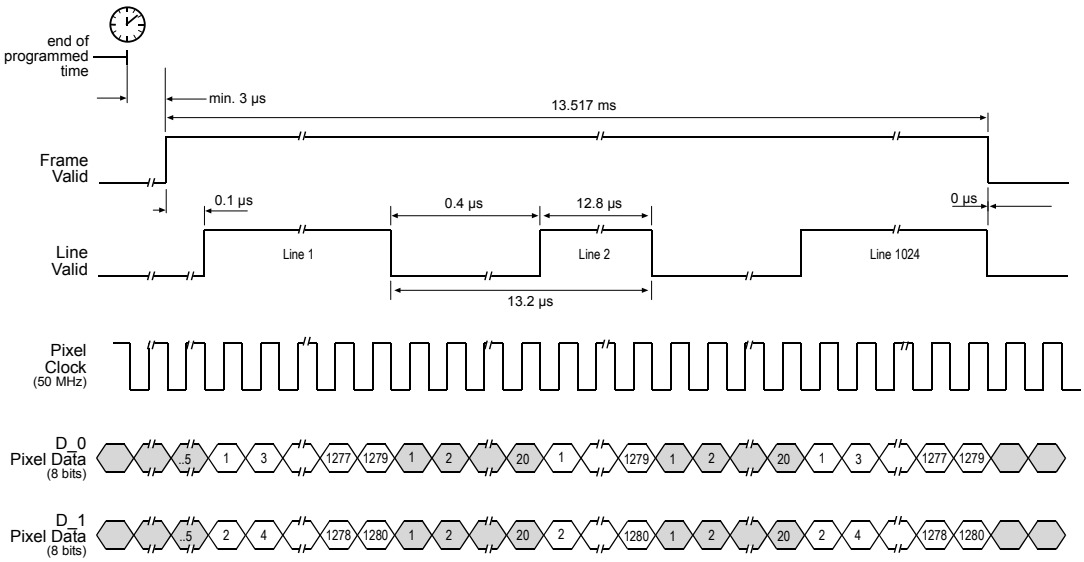
- This pattern will continue until all of the pixel data for each data stream for line one has been transmitted. (A total of 640 cycles for the **A501k/kc**.)
- Line valid becomes low for twenty pixel clocks.
- On the pixel clock cycle where data transmission for line two begins, the line valid bit will become high. Two data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the first and second pixel of line number two.
- On the next cycle of the pixel clock, the line valid bit will be high. Two data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the third and fourth pixel of line number two.
- On the next cycle of the pixel clock, the line valid bit will be high. Two data streams are transmitted in parallel during this clock cycle. In each data stream, 8 bits will contain the data for the fifth and sixth pixel of line number two.
- This pattern will continue until all of the pixel data for each data stream for line two has been transmitted. (A total of 640 cycles.)
- After all of the pixels in line two have been transmitted, the line valid bit will become low for twenty cycles indicating that valid data for line two is no longer being transmitted.
- The camera will continue to transmit pixel data for each line as described above until all of the lines in the frame have been transmitted. After all of the lines have been transmitted, the frame valid bit will become low at the same time as line valid indicating that a valid frame is no longer being transmitted.
- Frame valid will remain low for at least 15 pixel clock cycles until the next frame starts.

Figure 2-12 shows the data sequence when the camera is operating in edge-controlled or level-controlled exposure mode and Figure 2-13 shows the data sequence when the camera is operating in programmable exposure mode.



This diagram assumes that the area of interest feature is not being used. With the area of interest feature enabled, the number of pixels transferred could be smaller.

Figure 2-12: 8 Bit Output Mode with Edge or Level-controlled Exposure for the A501k/kc



This diagram assumes that the area of interest feature is not being used. With the area of interest feature enabled, the number of pixels transferred could be smaller.

Figure 2-13: 8 Bit Output Mode with Programmable Exposure for the A501k/kc

2.5.8 Flash Trigger Signal

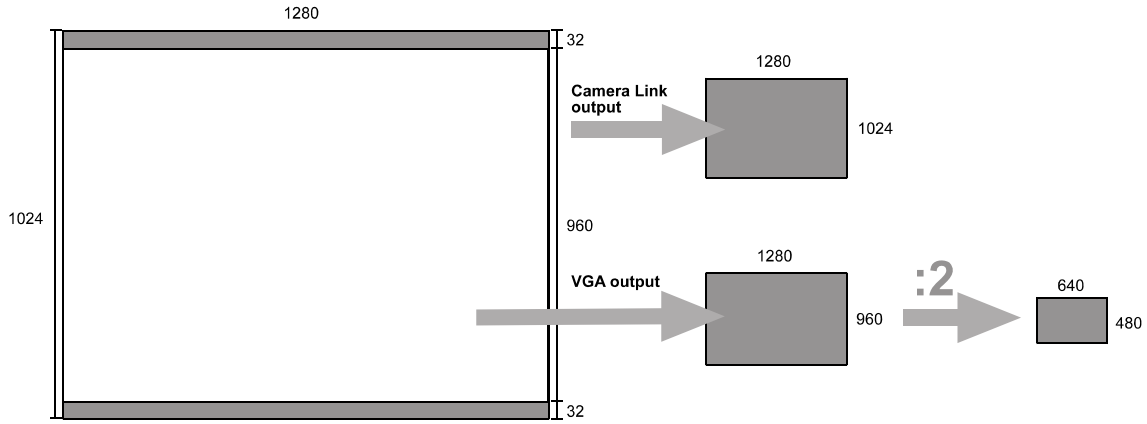
This signal can be programmed via the FlashCtrl register (see section 4.2.4.16). Six different options are programmable:

- The FlashOut trigger signal can be deactivated, that is, be set to low.
- It can be tied to an “effective exposure“ signal (Integrate Enabled) generated internally. This means that the FlashOut signal goes high when effective exposure starts and it goes low when effective exposure stops, regardless of the exposure mode chosen. As an option, the polarity of FlashOut can be inverted.
- The signal can be tied to the external ExFlash input signal provided by the framegrabber. As an option, the polarity of FlashOut can be inverted.
- FlashOut can be permanently high.

2.5.9 VGA Monitor Output (A504k/kc Only)

The VGA monitor output transmits 640 x 480 pixels RGB at a rate of 60 Hz. To achieve this, the image from the sensor (1280 x 1024 pixels) must be reduced. The first 32 lines and the last 32 lines of the image are not transmitted. Then, only every second pixel from the remaining 1280 x 960 pixels are transmitted to the VGA monitor output. The image on the monitor has a resolution of 640 x 480 pixels.

To activate the VGA monitor output, the free-run VGA exposure mode must be selected. The VGA exposure mode can only be used with a synchronous timing. In addition, it can only be operated in free-run, which means that it can NOT be triggered externally. The data is output at the VGA monitor connector and, at the same time, at the Camera Link output connectors.



When the camera is set to an exposure mode other than free-run VGA, a test image is output to the VGA output. The test image consists of monochrome gray wedges for monochrome cameras, or color wedges for color cameras.

Timing

The VGA exposure mode operates in a synchronous timing because the sensor timing must be adapted to the frame and line frequencies required by the monitor. In synchronous timings, the start of exposure is only possible at the falling edge of the line valid signal. In the VGA exposure mode, this fixed time pattern continues even while frame valid and line valid are low. The line valid signal period is 15.8 µs, so effective exposure is only possible in multiples of 15.8 µs, also while line valid is low. Frame valid rises 34 µs after the internal control signal has risen. See Figure 2-14.

If the exposure time is set so that the exposure start signal falls exactly onto the end of a high line valid signal, the effective exposure can jitter by 15.8 µs. To avoid this, change the exposure time by 1 µs.

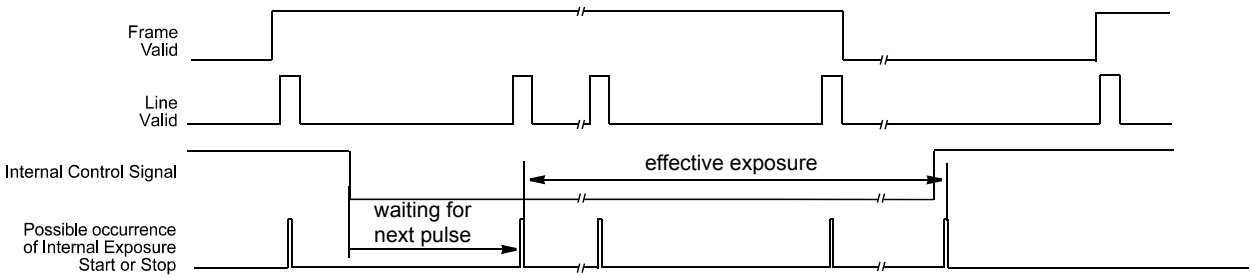


Figure 2-14: Output of VGA Exposure Mode

2.6 RS-644 Serial Communication

The **A500k** is equipped for RS-644 serial communication via the frame grabber as specified in the Camera Link standard. The RS-644 serial connection in the Camera Link interface is used to issue commands to the camera for changing modes and parameters. The serial link can also be used to query the camera about its current setup.

The Basler Camera Configuration Tool Plus (CCT+) is a convenient, graphical interface that can be used to change camera modes and parameters via the serial connection. The configuration tool is installed as part of the camera installation procedure shown in the booklet that is shipped with the camera. Section 4.1 provides some basic information about the configuration tool. Detailed instructions for using the tool are included in the on-line help file that is installed with the tool.

Basler has also developed a binary command protocol that can be used to change camera modes and parameters directly from your own application via the serial connection. See section 4.2 for details on the binary command format, and section 4.2 for information on how to configure the camera with binary commands.

2.6.1 Making the Serial Connection

Frame grabbers compliant with the Camera Link specification are equipped with a serial port integrated into the Camera Link interface that can be used for RS-644 serial communication. The characteristics of the serial port can vary from manufacturer.

If you are using the Basler CCT+ to configure the camera, the tool will detect the characteristics of the serial port on the frame grabber and will determine the appropriate settings so that the tool can open and use the port.

If you are configuring the camera using binary commands from within your application software, your software must be able to access the frame grabber serial port and to determine the appropriate settings so that it can open and use the port. See your frame grabber's documentation to determine the port access method and the port characteristics.

In order for the Camera Configuration Tool Plus and the CPA driver to detect and use the port, the characteristics of the port must comply with the Camera Link standard and the DLL called for in the standard must be present.

2.7 Converting Camera Link Output to RS-644 with a k-BIC (A501k/kc Only)

On the **A501k/kc**, video data is output from the camera in Camera Link LVDS format and parameter change commands are issued to the camera using RS-644 serial communication via the frame grabber. On older cameras, video data was output using an RS-644 LVDS format and commands were issued using RS-232 serial communication via the host PC. The output from **A501k/kc** cameras can be converted to the older style of output by using a Basler Interface Converter for k-series cameras (k-BIC). The k-BIC is a small device which attaches to the **A501k/kc** with a Camera Link compatible cable. For complete information on the k-BIC, refer to the k-BIC Users Manual and the k-BIC Installation Guide.

2.8 DC Power

The **A500k** requires 12 VDC (± 10%) power. The maximum power consumption is 6 W for the **A504k/kc**, 5.4 W for the **A503k/kc**, and 3 W for the **A501k/kc**. The current during constant operation is 500 mA max. for the **A504k/kc**, 450 mA max. for the **A503k/kc**, and 250 mA max. for the **A501k/kc**. Peak currents may occur. We recommend using 1.5 A power supplies.

The camera is equipped with an undervoltage lockout. The camera has no overvoltage protection.

Ripple must be less than 1%.

Caution!

Making or breaking connections when power is on can result in damage to the camera.

Be sure that all power to your system is switched off before you make or break connections to the camera.

If you can not switch off power, be sure that the power supply connector is the last connector plugged when you make connections to the camera, and the first connector unplugged when you break connections.

A Hirose plug will be shipped with each camera. This plug should be used to terminate the cable on the camera's power supply.

For proper EMI protection, the power supply cable attached to this plug must be a twin-core shielded cable. Also, the housing of the Hirose plug must be connected to the cable shield and the cable shield must be connected to earth ground at the power supply.

Make sure that the polarity is correct.

2.9 Power Control: Full Function and Standby

The camera can be set into a standby mode with register settings (see section 4.2.11). In standby mode, the camera's power consumption is reduced to 2.5 W for the **A504k/kc** and **A503k**, and 1.8 W for the **A501k/kc**. The Camera Link output is no longer fed, the sensor does not react any more. The monitor output available for the **A504k/kc** is no longer fed. The camera remembers the work set configuration. The serial communication is still operable. When the camera is set back to full function, it takes maximum 0.5 s until it is fully operable. During this startup time, the ExSync signal is not recognized reliably which can have the effect that the first image is not exposed correctly.

Power up time after power was off entirely takes a maximum of 3 s.

2.10 Status LED

When the LED on the back of the camera is not lit, it means that no power is present. When the LED is lit, it means that power to the camera is present.

Keep in mind that the circuit used to light the LED on the camera does not perform a voltage range check. If power to the camera is present but it is out of range, the LED on the camera may be lit but the camera will not operate properly.

When the LED on the back of the camera is orange this indicates signal integrity. At power up, the LED will light for several seconds in orange and sometimes green as the microprocessor in the camera boots up. If all is OK, the LED will then remain orange continuously.

If an error condition is detected at any time after the microprocessor boots up, the LED will begin flashing an error code. See section 6 for details.

3 Basic Operation and Features

3.1 Functional Description

BASLER A500k area scan cameras employ a CMOS-sensor chip which provides features such as a full frame shutter, electronic exposure time control and anti-blooming. Exposure time is controlled either internally via an internal sync signal (free-run mode) or externally via an external trigger (ExSync) signal. The ExSync signal facilitates periodic or non-periodic pixel readout.

In any free-run mode, the camera generates its own internal control signal and the internal signal is used to control exposure and charge read out. When operating in free-run, the camera outputs frames continuously.

The internally generated “effective exposure“ signal (Integrate Enabled) can be tied to the FlashOut signal (see sections 2.1.4 and 4.2.4.16).

When exposure is controlled by an ExSync signal, exposure time can be either edge-controlled, level-controlled or programmable. In edge-controlled mode, charge is accumulated from the rising edge to the next rising edge of ExSync. The rising edge of ExSync also triggers the readout. In level-controlled mode, charge is accumulated when the ExSync signal is low and a rising edge of ExSync triggers the readout. In programmable mode, exposure time can be programmed to a predetermined time period. In this case, exposure begins on the rising edge of ExSync and accumulated charges are read out when the programmed exposure time ends.

The **A504k/kc** has a special feature: In addition to sending video data to a framegrabber, it can be output to an VGA monitor (640 x 480 pixels). In VGA exposure mode the camera generates its own internal control signal and the internal signal is used to control exposure and charge read out. The frame frequency is set to 60 Hz. The camera outputs frames continuously to the monitor and, at the same time, to the Camera Link output.

At readout, for **A500k** series cameras, all accumulated charges of all pixels are simultaneously transported from the light-sensitive sensor elements (pixels) to the pixel memory (full frame shutter). There is a pixel memory for each pixel. As a consequence, the camera can be exposed and read out at the same time. The charges of the pixel memory are amplified. The pixel memories can be connected to a bus. There is one bus for each vertical column. At the end of each bus, there is an analog/digital converter (ADC).

For readout, the pixel memories can be addressed linewise by closing a switch that connects the pixel memory of the addressed lines to the busses. Before the analog video data enters the ADC, the offset is added, plus a value that corrects column fixed pattern noise. The analog video data is digitized by a ten bit, Analog to Digital converter (ADC). The ADC’s reference value is used to set the gain. The digitized video data then passes a digital 128 stage shift register, which outputs 10 x 10 Bit of data in parallel with each cycle. Then the 10 Bit sensor output enters the digital shifter

in the FPGA if 8 bit output is selected. The digital shifter selects the most significant 8 bits out of the 10 bits for the **A504k/kc, A503k,** and **A501k/kc**.

In the next step, different data flows occur:

- In the **A504k/kc**, the data is formatted to be output in 10 parallel data streams (10 taps).
- In the **A503k**, the data is formatted to be output in 8 parallel data streams (8 taps)
- In the **A501k/kc,** the data is formatted to be output in 2 parallel data streams (2 taps).

The 8 Bit video data per pixel is transmitted from the camera to the frame grabber using a Camera Link transmission format (see section 2.5 for details).

For optimal digitization, gain and offset are programmable via a serial port.

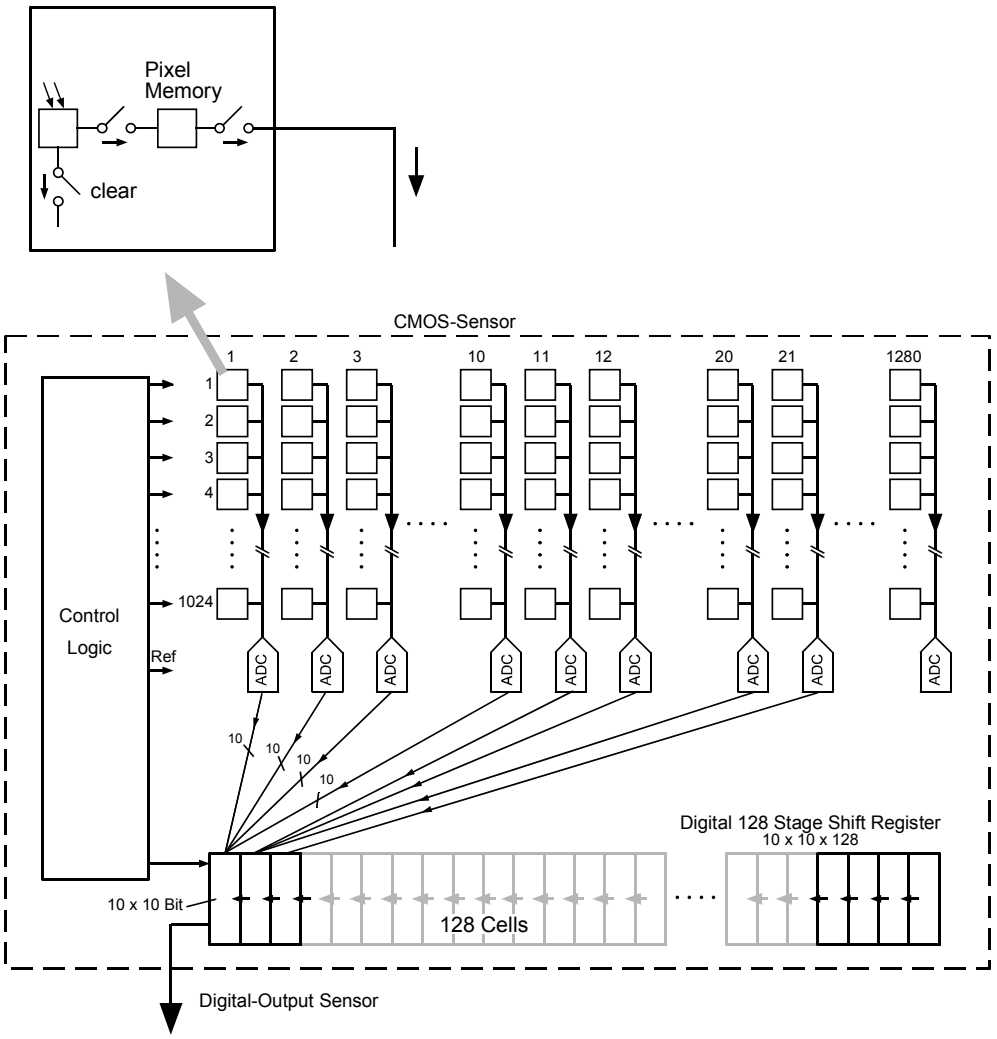


Figure 3-1: **A500k/kc** Sensor Architecture

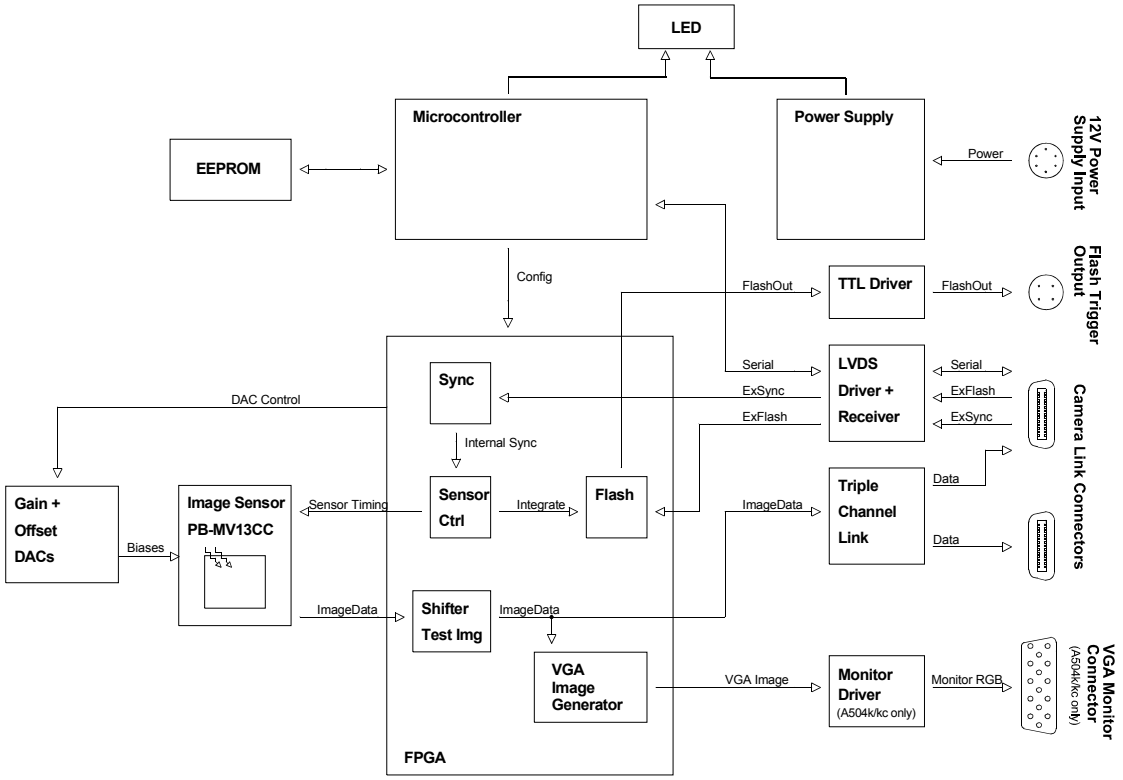


Figure 3-2: **A504k/kc**, **A503k** Block Diagram

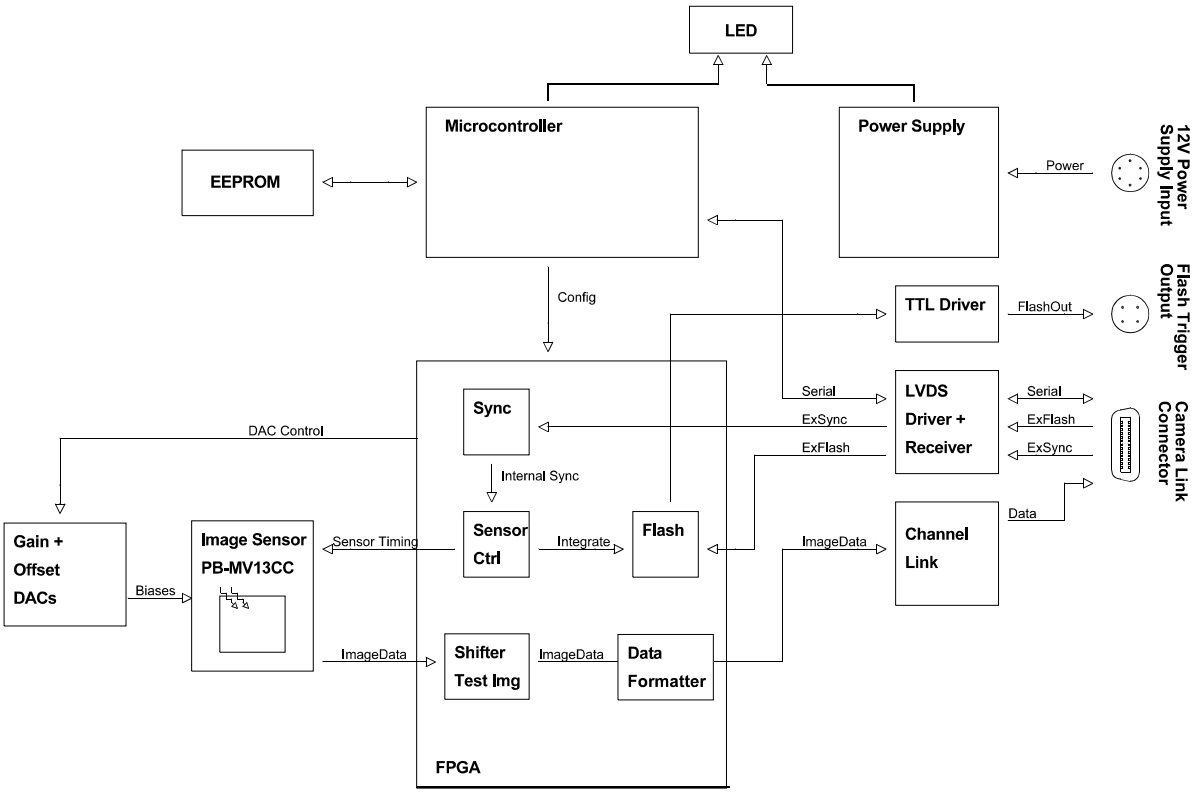


Figure 3-3: **A501k/kc** Block Diagram

3.2 Exposure Time Control Modes

A500k cameras can operate under the control of an external trigger signal (ExSync signal) or can operate in “free-run.” In free-run, the camera generates its own internal control signal and does not require an ExSync signal.

3.2.1 ExSync Controlled Operation

In ExSync operation, the camera’s frame rate and exposure time are controlled by an externally generated (ExSync) signal. The ExSync signal is typically supplied to the camera by a frame grabber board. You should refer to the manual supplied with your frame grabber board to determine how to set up the ExSync signal that is being supplied to the camera.

When the camera is operating under the control of an ExSync signal, the length of the ExSync signal period determines the camera’s frame rate. ExSync can be periodic or non-periodic.

When the camera is operating with an ExSync signal, it has three modes of exposure time control available: edge-controlled mode, level-controlled mode and programmable mode.

- In **ExSync**, **edge-controlled** mode, the pixels are exposed and charge is accumulated over the full period of the ExSync signal (rising edge to rising edge). The falling edge of the ExSync signal is not relevant. The frame is read out and transferred on the rising edge of ExSync (see Figure 3-4).

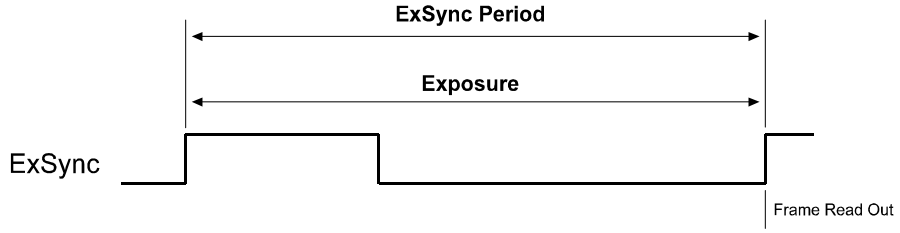


Figure 3-4: ExSync, Edge-controlled Mode

- In **ExSync**, **level-controlled** mode, the exposure time is determined by the time between the falling edge of ExSync and the next rising edge. The pixels are exposed and charge is accumulated only when ExSync is low. The frame is read out and transferred on the rising edge of the ExSync signal (see Figure 3-5).

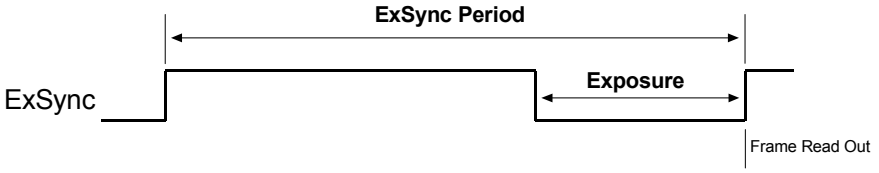


Figure 3-5: ExSync, Level-controlled Mode

- In **ExSync**, **programmable** mode, the rising edge of ExSync triggers exposure and charge accumulation for a pre-programmed period of time. The frame is read out and transferred at the end of the pre-programmed period. The falling edge of ExSync is not relevant (see Figure 3-6).

  A parameter called the “Timer 1” is used to set the length of the pre-programmed exposure period.

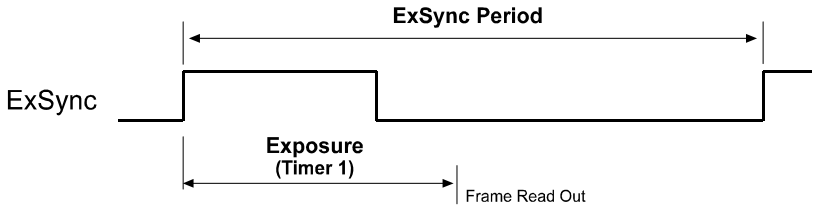


Figure 3-6: ExSync, Programmable Mode

If you want to operate the camera at maximum exposure time and maximum frame rate, see section 3.5 for further setting recommendations.

You can set the camera to operate in one of the ExSync controlled exposure modes using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2).

With the Camera Configuration Tool Plus, you use the Exposure Time Control Mode command to set the camera for ExSync operation and to select the level controlled or programmable exposure time control mode. If you select the programmable mode, you must also enter an exposure time. When you enter an exposure time, the configuration tool will automatically set the “Timer 1” parameter to the correct value.

With binary commands, you must use the Exposure Time Control Mode command to select ExSync level-controlled or ExSync programmable mode. If you choose the programmable mode, you must also use the Timer 1 command to set the exposure time.

3.2.2 Free Run

In **free-run**, no ExSync signal is required. The camera generates a continuous internal control signal.

When the camera is operating in free-run, it exposes and outputs frames continuously.

A500k cameras have a free-run, programmable mode. The **A504k/kc** cameras additionally have a free-run, VGA mode.

- In **free-run**, **programmable mode**, the camera generates a continuous internal control signal based on two programmable parameters: “Timer 1” and “Timer 2.” Timer 1 determines how long the internal control signal will remain low and Timer 2 determines how long the signal will remain high. Pixels are exposed and charge is accumulated when the internal control signal is low. The length of the control signal period determines the camera’s frame rate. The control signal period is equal to Timer 1 plus Timer 2. The frame is read out and transferred on the rising edge of the internal control signal. See Figure 3-7.

  In this mode, the exposure time can programmed as desired by varying the setting of the “Timer 1” parameter.

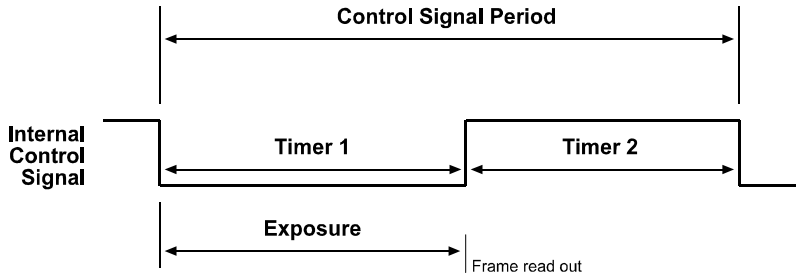


Figure 3-7: Free-run, Programmable Mode

	In the free-run programmable mode, the period of the internal control signal is equal to the sum of Timer 1 plus Timer 2. The sum of the Timer 1 setting plus the Timer 2 setting must be greater than the maximum frame rate. The minimum exposure time is 10 µs.

- In **free-run**, **VGA mode (A504k/kc** only), the camera generates a continuous internal control signal which is set to 60 Hz and can not be varied. The data is output at the VGA monitor output connector and at the Camera Link connectors. Timer 1 determines how long the internal signal will remain low. Pixels are exposed and charge is accumulated when the internal control signal is low. In this mode, the exposure time can be programmed as desired by varying the setting of the “Timer 1” parameter.

  The minimum exposure time is 10 µs.

  Also see section 2.5.9 for a description of the VGA monitor output mode.

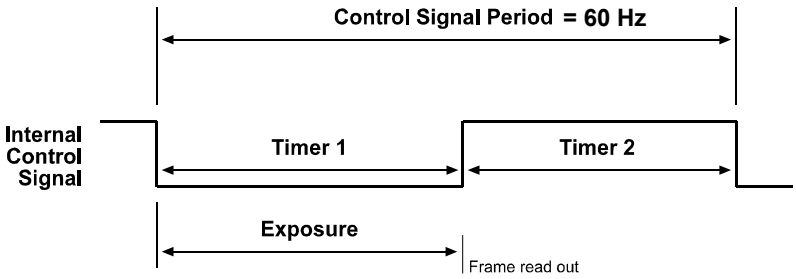


Figure 3-8: Free-run, VGA Mode

If you want to operate the camera at maximum exposure and maximum frame rate, see section 3.5 for further setting recommendations.

You can set the camera to operate in free-run using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2).

With the Camera Configuration Tool Plus, you use the Exposure Time Control Mode command to set the camera for free-run and to select the edge-controlled or programmable exposure time control mode. If you choose to operate the camera in free-run, the configuration tool will require you to enter a frame rate; if you are using the programmable mode, you must also enter an exposure time. The configuration tool will automatically set the Timer 1 and Timer 2 parameters based on the values that you enter on the Exposure Tab.

With binary commands you must use the Exposure Time Control Mode command to select the free-run, programmable or free-run, VGA mode. You must also use the Timer 1 command to set Timer 1 and the Timer 2 command to set Timer 2.

3.3 Exposure Time Control Modes in Detail

This section is aimed at system integrators or engineers who intend to develop their own framegrabbers or preprocessing. If you are using a commercially available framegrabber, the framegrabber takes care of the different timings described in this section without the need for any action by you.

Depending on the frame rate and exposure time determined by setting the ExSync signal or the Timer 1 and Timer 2 values, the timing of the exposure control signals differs. There are four different timings and the camera switches between these four timings **automatically**. The timings are labelled asynchronous timing, synchronous/asynchronous timing, synchronous timing 1, and synchronous timing 2.

Asynchronous timing operates the camera with “non-overlapped“ exposure. In this case each time a frame is captured, the camera completes the entire exposure/readout process before capture of the next frame is triggered.

Synchronous/asynchronous timing, synchronous timing 1, and synchronous timing 2 operate the camera with „overalapped“ exposure. In this case the exposure of frame N+1 is triggered before the readout of frame N is complete.

This introductory section contains formulas that describe the conditions for the camera to enter the four timings. The formulas were generalized as much as possible, but the figures were taken from the Free-run mode. They can be different in other exposure time control modes.

For detailed information, see the detailed timings described in sections 3.3.1 through 3.3.4.

Frame Valid High is 2000 µs for the **A504k/kc**, 2485 µs for the **A503k** and 13.517 ms for the **A501k/kc**.

$$\text{Frame Period} = \frac{1}{\text{Frame Rate}}$$

- **Asynchronous Timing:** This is the slowest timing. This timing is always used for the first image. You can realize a long exposure time with this timing. Exposure and readout are performed sequentially. Exposure of frame N+1 starts after readout of frame N while frame valid is low. Readout of frame N+1 is triggered after readout of frame N while frame valid is low.
  To let the camera operate in this timing, set the frame rate and the exposure time so that the following condition is met:

  Frame Period > Exposure Time + Frame Valid High

  The asynchronous timing is described in more detail in sections 3.3.1.1, 3.3.2.1, 3.3.3.1, and 3.3.4.1 for each exposure mode.

  Synchronous/Asynchronous Timing: This timing is suitable for long exposure times. Exposure of frame N+1 starts during readout of frame N while frame valid is high. Readout of frame N+1 is triggered after readout of frame N while frame valid is low.
  To let the camera operate with this timing, set the frame rate and the exposure time so that the following conditions are met:

  Frame Period < Exposure Time + Frame Valid High

  Frame Period > Frame Valid High + 3 µs for A504k/kc (or 3.75 µs for A503k or 20.2 µs for A501k/kc)

The synchronous/asynchronous timing is described in sections 3.3.2.2, 3.3.3.2, and 3.3.4.2 for each exposure mode.

Synchronous Timing 1: The time that frame valid is low between two subsequent frames corresponds to the time of one and a half lines. Exposure of frame N+1 starts during readout of frame N while frame valid is high. Readout of frame N+1 is triggered during transmission of the last line of frame N, i.e. while frame valid and line valid of the last line are high.
To let the camera operate with this timing, set the frame rate and the exposure time that the following conditions are met:

Frame Period < Frame Valid High + 3 µs for A504k/kc (or 3.75 µs for A503k or 20.2 µs for A501k/kc)

Frame Period > Frame Valid High + 44 ns for A504k/kc (or 60 ns for A503k or 300 ns for A501k/kc)

The synchronous timing 1 is described in sections 3.3.1.2, 3.3.2.3, 3.3.3.3, and 3.3.4.3 for each exposure mode.

- **Synchronous Timing 2:** This is the fastest timing. Frame valid is low for 3 (**A504k/kc**) or 4 (A503k) or 15 (**A501k/kc**) pixel clocks between two subsequent frames. Exposure of frame N+1 starts during readout of frame N while frame valid is high. Readout of frame N+1 is triggered during readout of the next to the last line of frame N, i.e. while frame valid is high and line valid of the next to the last line is high. To let the camera operate with this timing, set the frame rate and the exposure time that the following conditions are met:

  Frame Period < Frame Valid High + 44 ns for A504k/kc (or 60 ns for A503k or 300 ns for A501k/kc)

  $$\text{Frame Period} \geq \frac{1}{\text{Max. Frame Rate}}$$

  The synchronous timing 2 is described in sections 3.3.1.3, 3.3.2.4, 3.3.3.4, and 3.3.4.4 for each exposure mode. Also see section 3.5 on how to set frame rate and exposure time to achieve this exposure mode at full AOI.

The following sections describe the detailed timing of the exposure time control modes depending on the selected frame rate and exposure time.

	The following values are valid for all timing diagrams: ExSync drives the internal camera control signal. The internal control signal takes less than 200 ns to react to ExSync in the **A504k/kc** and **A503k/kc**, and less than 1 µs in the **A501k/kc**. The minimum exposure time is 10 µs for all modes. Line valid rises after frame valid has risen (see Figure 2-8 to Figure 2-13).

	The following timing diagrams all show an Integrate Enabled signal: The Integrate Enabled signal is high during effective exposure, i.e. when charges are actually accumulated by the sensor. The FlashOut signal can be tied to the Integrate Enabled signal and transmitted out of the camera (see section 2.1.4).

3.3.1 ExSync, Edge-controlled Mode

When using the ExSync edge-controlled mode to control exposure, several guidelines must be followed:

- ExSync must remain high for a minimum of 1 µs.
- ExSync must remain low for a minimum of 1 µs.
- When using full resolution, the minimum ExSync period is 2 ms for the **A504k/kc**, 2.485 ms for the **A503k** and 13.52 ms for the **A501k/kc**.
- If the AOI feature is used, the minimum ExSync signal period is equal to 1/Maximum Frame Rate where the maximum frame rate is determined by the suitable formula in section 3.11.1.

Assuming that these general guidelines are followed, the reaction of the camera to a rising ExSync signal will be one of three cases, which are described in sections 3.3.1.1, 3.3.1.2 and 3.3.1.3.

The FlashOut signal can be set into a mode where it is high while the effective exposure occurs, i.e. while the Integrate Enabled signal is high.

3.3.1.1 ExSync, Edge-controlled Mode with Asynchronous Timing

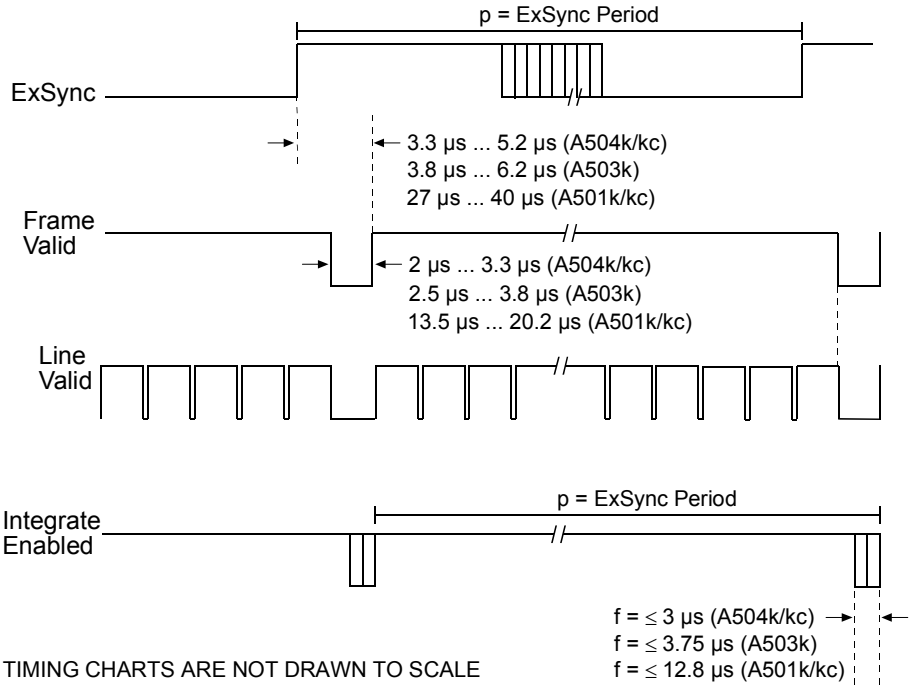


Figure 3-9: ExSync, Edge-controlled Mode - Exposure Start and Stop with Frame Valid Low

The ExSync signal goes high and goes low while the Frame Valid signal is low. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-9):

- The effective exposure starts d microseconds after the rise of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by the ExSync period p.
- The effective exposure stops d microseconds or less (see following item) after the consecutive rise of the ExSync signal.
- Jitter (f) may shorten the effective exposure, i.e.
  duration of the effective exposure = p - f .

Due to the propagation time of approximately 1 µs, ExSync can go high up to 1 µs before frame valid goes low.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by ExSync		
d	3.3 µs	3.8 µs	20.8 µs
f	≤ 3 µs	≤ 3.5 µs	≤ 12.8 µs

3.3.1.2 ExSync, Edge-controlled Mode with Synchronous Timing 1

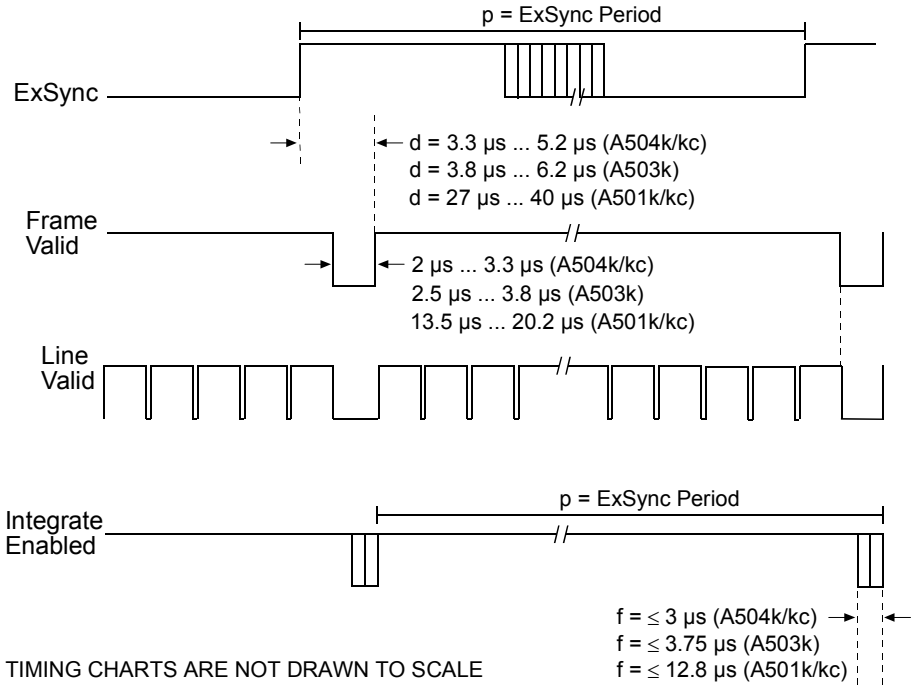


Figure 3-10: ExSync, Edge-controlled Mode - Exposure Start and Stop with Frame Valid High

The ExSync signal goes high and goes low while the Frame Valid signal is high. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-10):

- The effective exposure starts d microseconds after the rise of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by the ExSync period p.
- The effective exposure stops d microseconds or less (see following item) after the consecutive rise of the ExSync signal.
- Jitter (f) may shorten the effective exposure, i.e.
  duration of the effective exposure = p - f.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by ExSync		
d	3.3 ... 5.2 µs	3.8 ... 6.2 µs	27 ... 40 µs
f	≤ 3 µs	≤ 3.75 µs	≤ 12.8 µs

3.3.1.3 ExSync, Edge-controlled Mode with Synchronous Timing 2

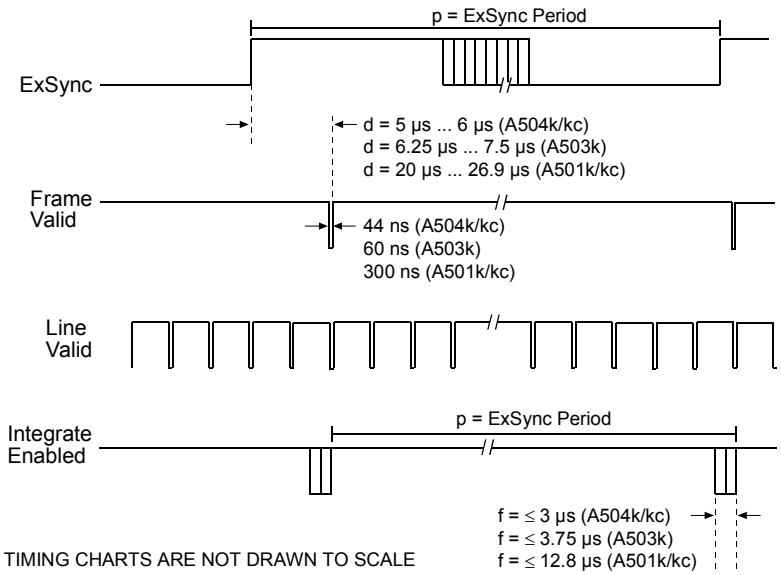


Figure 3-11: ExSync, Edge-controlled Mode - Exposure Start and Stop with Frame Valid High

The ExSync signal goes high and goes low while the Frame Valid signal is high. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-11):

- The effective exposure starts d microseconds after the rise of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by the ExSync period p.
- The effective exposure stops d microseconds or less (see following item) after the consecutive rise of the ExSync signal.
- Jitter (f) may shorten the effective exposure, i.e.
  duration of the effective exposure = p - f.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by ExSync		
d	5 µs ... 6 µs	6.25 µs ... 7.5 µs	20 ... 26.9 µs
f	≤ 3 µs	≤ 3.75 µs	≤ 12.8 µs

3.3.2 ExSync, Level-controlled Mode

When using the ExSync level-controlled mode to control exposure, several guidelines must be followed:

- ExSync must remain high for a minimum of 5 µs.
- ExSync must remain low for a minimum of 10 µs.
- When using full resolution, the minimum ExSync signal period is 2 ms for the **A504k/kc**, 2.485 ms for the **A503k**, and 13.52 ms for the **A501k/kc**.
- If the AOI feature is used, the minimum ExSync signal period is equal to 1/Maximum Frame Rate where the maximum frame rate is determined by the suitable formula in section 3.11.1.

Assuming that these general guidelines are followed, the reaction of the camera to a falling ExSync signal will be one of four cases, which are described in sections 3.3.2.1, 3.3.2.2, 3.3.2.3 and 3.3.2.4.

The FlashOut signal can be set into a mode where it is high while the effective exposure occurs, i.e. while the Integrate Enabled signal is high.

3.3.2.1 ExSync, Level-controlled Mode with Asynchronous Timing

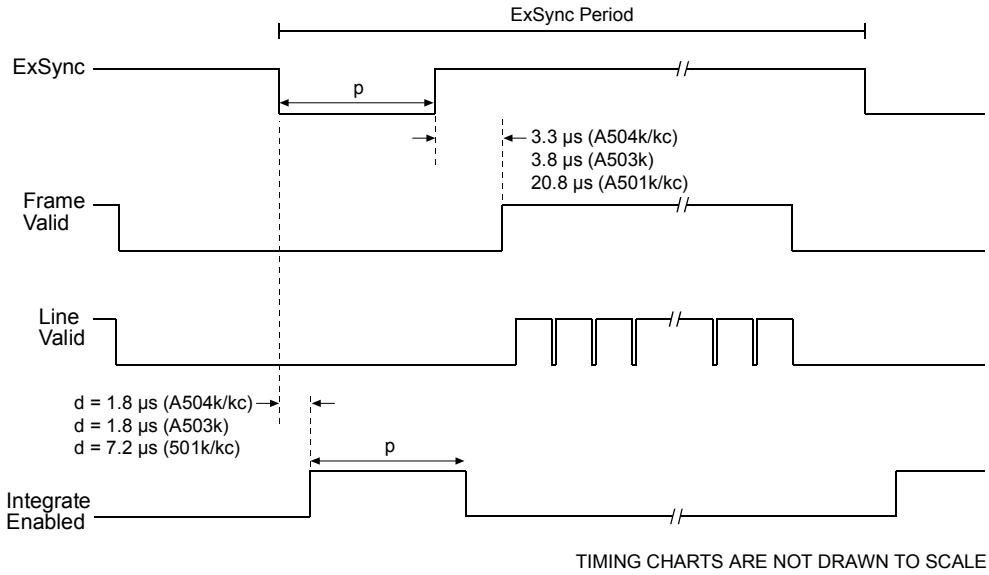


Figure 3-12: ExSync, Level-controlled Mode - Exposure Start and Stop when Frame Valid is Low

The ExSync signal goes low and goes high while the Frame Valid signal is low. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-12):

- The effective exposure starts d microseconds after the fall of the ExSync signal (exposure start delay).
- The duration of the effective exposure is defined by period p.
- The effective exposure stops d microseconds after the rise of the ExSync signal.

ExSync signal can already go low up to 1 µs before Frame Valid is low.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by ExSync		
d	1.8 µs	1.8 µs	7.2 µs

3.3.2.2 ExSync, Level-controlled Mode with Synchronous/Asynchronous Timing

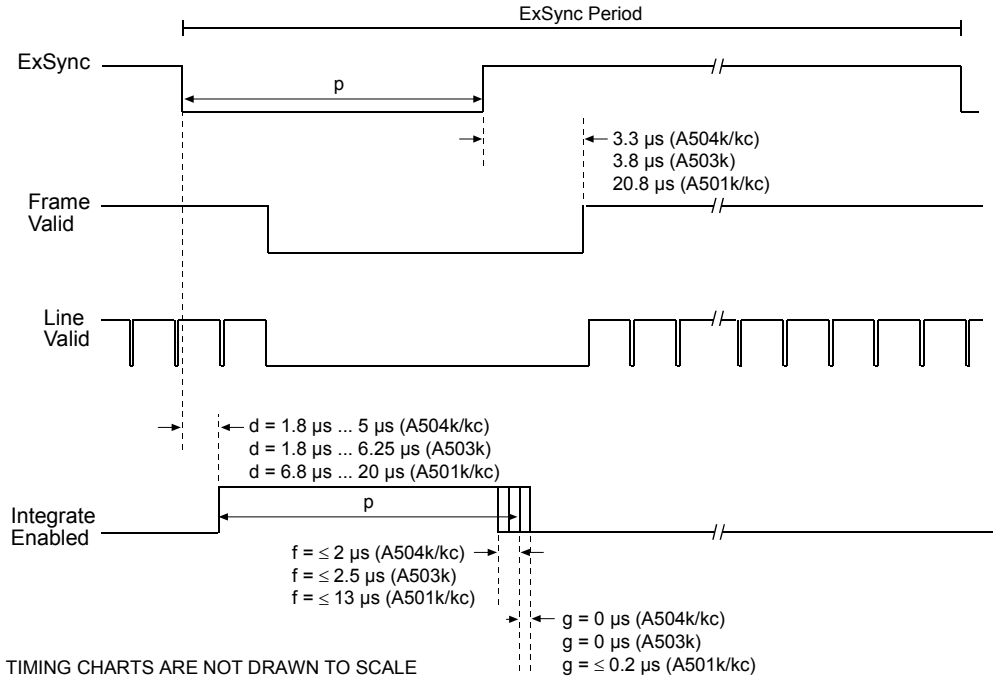


Figure 3-13: ExSync, Level-controlled Mode - Exposure Start when Frame Valid is High, Exposure Stop when Frame Valid is Low

The ExSync signal goes high while the Frame Valid signal is high and it goes low while the Frame Valid signal is low. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-13):

- The effective exposure starts d microseconds after the fall of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p.
- Jitter may shorten (f) or extend (g) the effective exposure, i.e.
  duration of the effective exposure = (p - f) to (p + g).

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by ExSync		
d	1.8 µs ... 5 µs	1.8 µs ... 6.25 µs	6.8 µs ... 20 µs
f	≤ 2 µs	≤ 2.5 µs	≤ 13 µs
g	0 µs	0 µs	≤ 0.2 µs

3.3.2.3 ExSync, Level-controlled Mode with Synchronous Timing 1

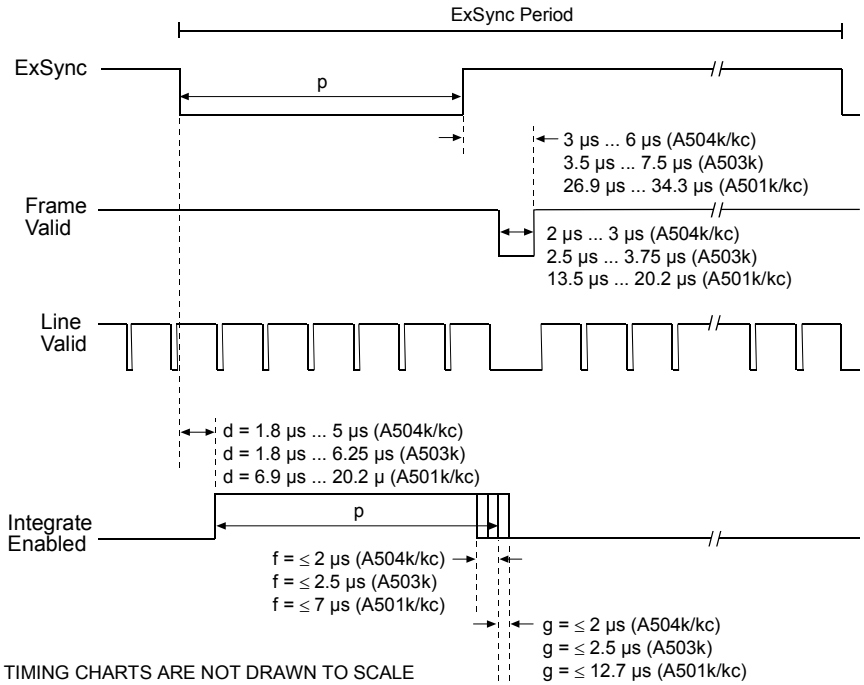


Figure 3-14: ExSync, Level-controlled Mode - Exposure Start and Stop when Frame Valid is High

The ExSync signal goes low and goes high while the Frame Valid signal is high. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-14):

- The effective exposure starts d microseconds after the fall of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p.
- Jitter may shorten (f) or extend (g) the effective exposure, i.e.
  duration of the effective exposure = (p - f) to (p + g).
- The duration of the effective exposure can only occur in multiples of m microseconds.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by ExSync		
d	1.8 µs ... 5 µs	1.8 µs ... 6.25 µs	6.9 µs ... 20.2 µs
f	≤ 2 µs	≤ 2.5 µs	≤ 7 µs
g	≤ 2 µs	≤ 2.5 µs	≤ 12.7 µs
m	2 µs	2.5 µs	13.2 µs

3.3.2.4 ExSync, Level-controlled Mode with Synchronous Timing 2

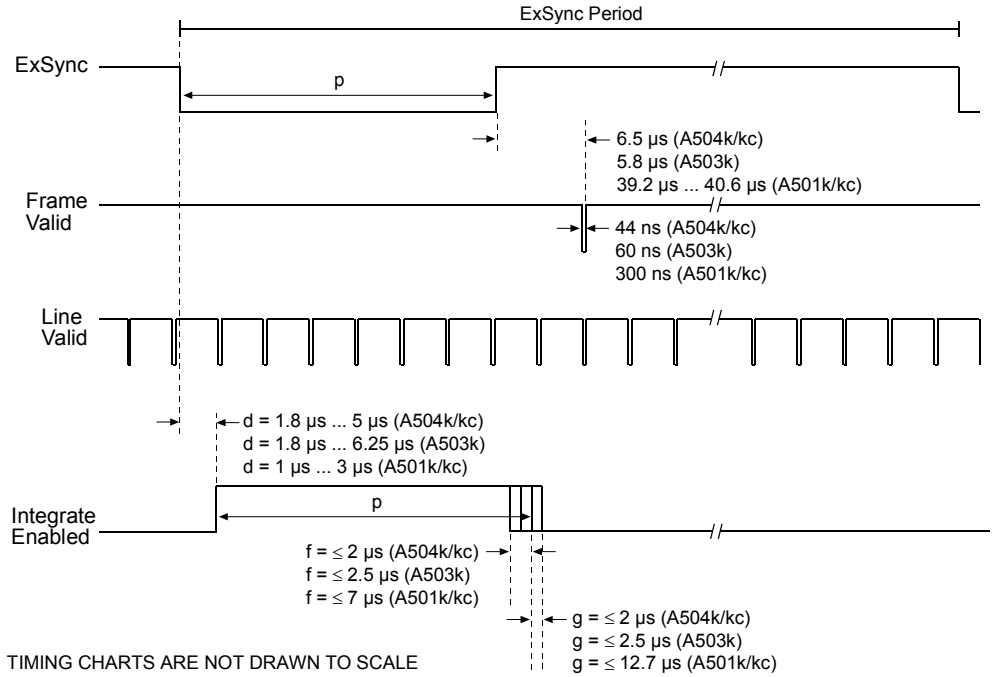


Figure 3-15: ExSync, Level-controlled Mode - Exposure Start and Stop when Frame Valid High

The ExSync signal goes low and goes high while the Frame Valid signal is high. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-15):

- The effective exposure starts d microseconds after the fall of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p.
- Jitter may shorten (f) or extend (g) the effective exposure, i.e.
  duration of the effective exposure = (p - f) to (p + g).
- The duration of the effective exposure can only occur in multiples of m microseconds.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by ExSync		
d	1.8 µs ... 5 µs	1.8 µs ... 6.25 µs	1 µs ... 3 µs
f	≤ 2 µs	≤ 2.5 µs	≤ 7 µs
g	≤ 2 µs	≤ 2.5 µs	≤ 12.7 µs
m	2 µs	2.5 µs	13.2 µs

3.3.3 ExSync, Programmable Mode

When using the ExSync programmable mode to control exposure, several guidelines must be followed:

- ExSync must remain high for a minimum of 1 µs.
- ExSync must remain low for a minimum of 1 µs.
- Timer 1 must be set to a minimum of 10 µs.
- Using full resolution, the minimum ExSync signal period is 2 ms for the **A504k/kc**, 2.485 ms for the **A503k** and 13.52 ms for the **A501k/kc**.
- If the AOI feature is used, the minimum ExSync signal period is equal to 1/Maximum Frame Rate where the maximum frame rate is determined by the suitable formula in section 3.11.1.

Assuming that these general guidelines are followed, the reaction of the camera to a falling ExSync signal will be one of four cases, which are described in sections 3.3.3.1, 3.3.3.2, 3.3.3.3 and 3.3.3.4.

The FlashOut signal can be set into a mode where it is high while the effective exposure occurs, i.e. while the Integrate Enabled signal is high.

3.3.3.1 ExSync, Programmable Mode with Asynchronous Timing

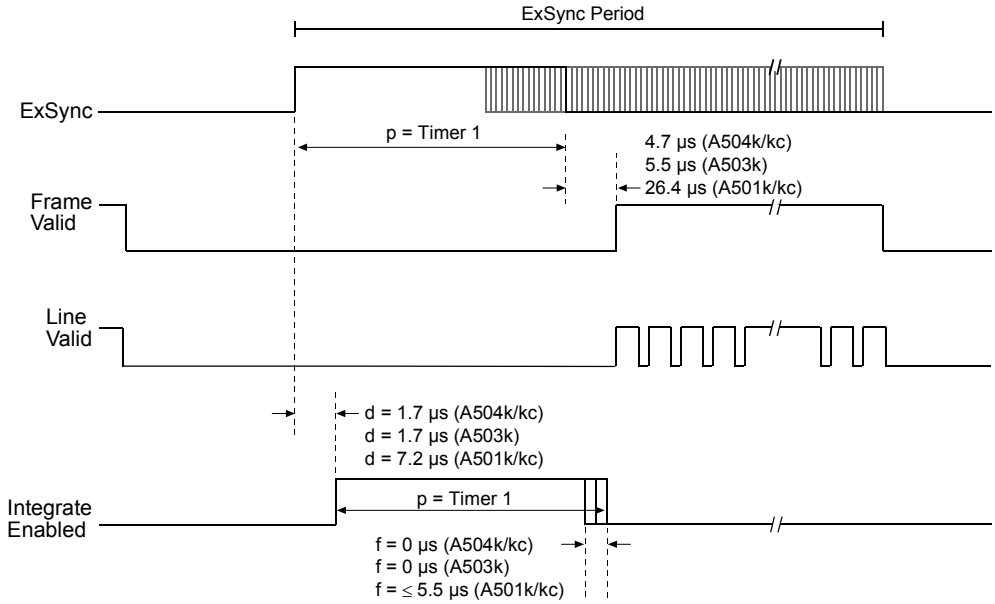


Figure 3-16: ExSync, Programmable Mode - Exposure Start and Stop with Frame Valid Low

The effective exposure occurs while the Frame Valid signal is low. The FlashOut signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-16):

- The effective exposure starts d microseconds after the rise of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter (f) may shorten the effective exposure, i.e. duration of the effective exposure = p - f .

Due to the propagation time of approximately 1 µs, ExSync can go high up to 1 µs before the Frame Valid signal goes low.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by Timer 1		
d	1.7 µs	1.7 µs	7.2 µs
f	0 µs	0 µs	≤ 5.5 µs

3.3.3.2 ExSync, Programmable Mode with Synchronous/Asynchronous Timing

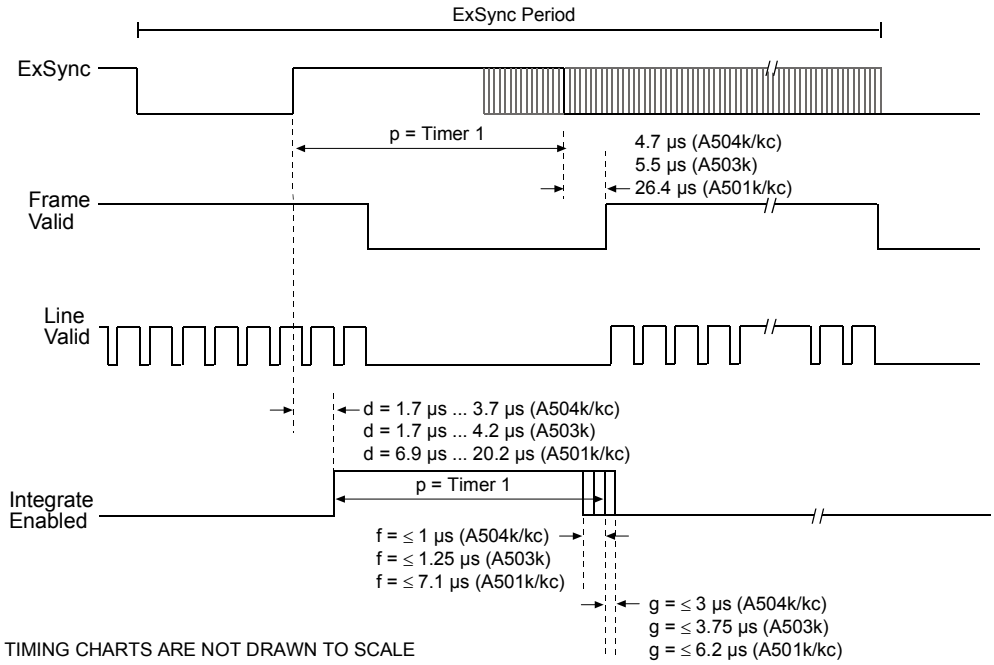


Figure 3-17: ExSync, Programmable Mode - Exposure Start When Frame Valid is High, Exposure Stop When Frame Valid is Low

The effective exposure starts while the Frame Valid signal is high and stops while the Frame Valid signal is low. The FlashOut signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-17):

- The effective exposure starts d microseconds after the rise of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter may shorten (f) or extend (g) the effective exposure, i.e. duration of the effective exposure = p - f.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by Timer 1		
d	1.7 µs ... 3.7 µs	1.7 µs ... 4.2 µs	6.9 µs ... 20.2 µs
f	≤ 1 µs	≤ 1.25 µs	≤ 7.1 µs
g	≤ 3 µs	≤ 3.75 µs	≤ 6.2 µs

3.3.3.3 ExSync, Programmable Mode with Synchronous Timing 1

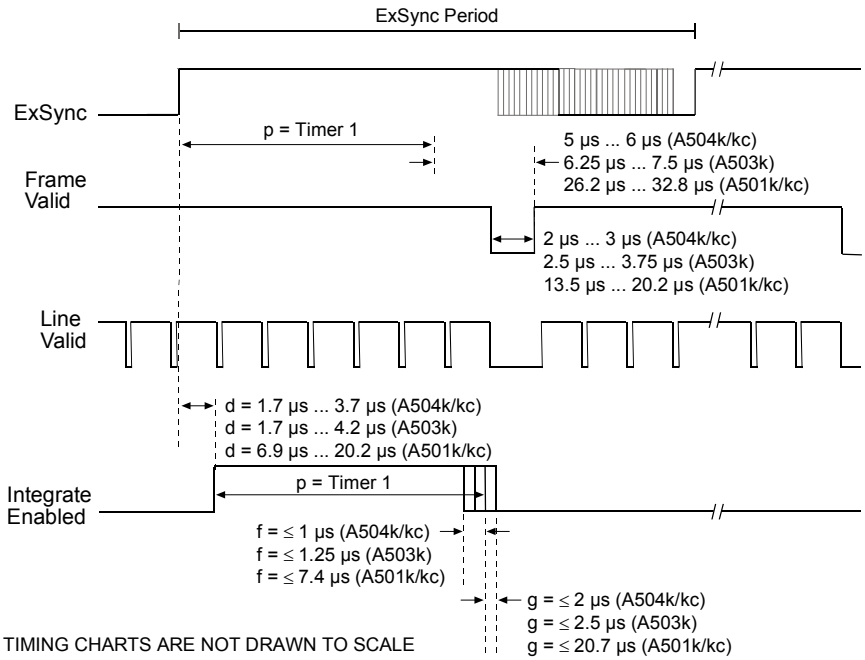


Figure 3-18: ExSync, Programmable Mode - Exposure Start and Stop When Frame Valid is High

The effective exposure starts and stops while the Frame Valid signal is high. The FlashOut signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-18):

- The effective exposure starts d microseconds after the rise of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter may shorten (f) or extend (g) the effective exposure, i.e.
  duration of the effective exposure = (p - f) to (p + g).
- The duration of the effective exposure can jitter by 1 µs and it can only occur in multiples of m microseconds.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by Timer 1		
d	1.7 µs ... 3.7 µs	1.7 µs ... 4.2 µs	6.9 µs ... 20.2 µs
f	≤ 1 µs	≤ 1.25 µs	≤ 7.4 µs
g	≤ 2 µs	≤ 2.5 µs	≤ 20.7 µs
m	2 µs	2.5 µs	13.2 µs

3.3.3.4 ExSync, Programmable Mode with Synchronous Timing 2

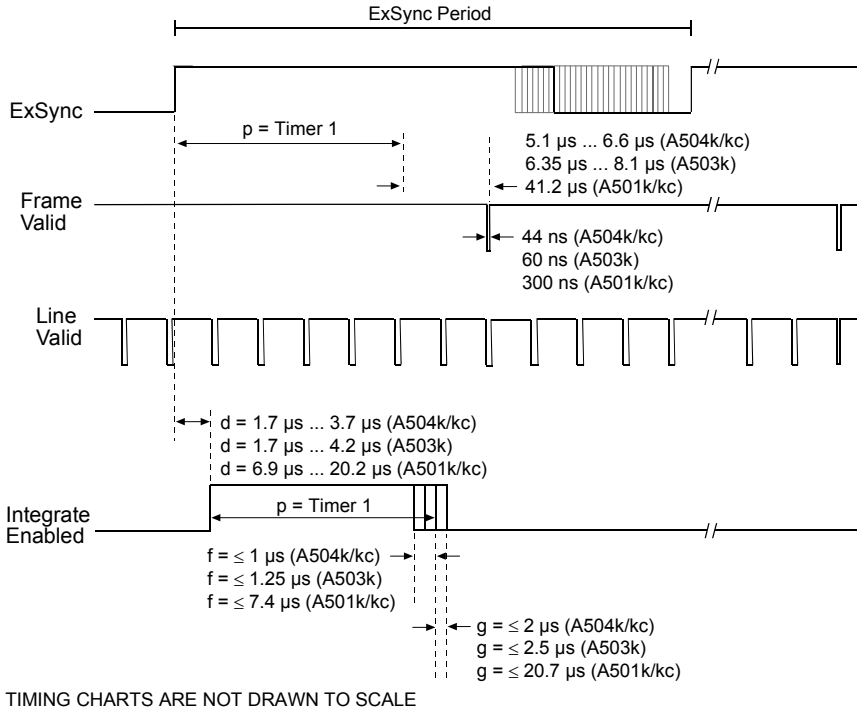


Figure 3-19: ExSync, Programmable Mode - Exposure Start and Stop with Frame Valid High

The effective exposure starts and stops while the Frame Valid signal is high. The FlashOut signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-19):

- The effective exposure starts d microseconds after the rise of the ExSync signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter may shorten (f) or extend (g) the effective exposure, i.e. duration of the effective exposure = (p - f) to (p + g).
- The duration of the effective exposure can only occur in multiples of m microseconds.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by Timer 1		
d	1.7 µs ... 3.7 µs	1.7 µs ... 4.2 µs	6.9 µs ... 20.2 µs
f	≤ 1 µs	≤ 1.25 µs	≤ 7.4 µs
g	≤ 2 µs	≤ 2.5 µs	≤ 20.7 µs
m	2 µs	2.5 µs	13.2 µs

3.3.4 Free-run Mode

When using the free-run, programmable mode to control exposure, several guidelines must be followed:

- The internal control signal must remain high for a minimum of 3 µs.
- The internal control signal must remain low for a minimum of 10 µs.
- Using full resolution, the minimum internal control signal period is 2 ms for the **A504k/kc**, 2.485 ms for the **A503k**, and 13.52 ms for the **A501k/kc**.
- If the AOI feature is used, the minimum internal control signal period is equal to 1/Maximum Frame Rate where the maximum frame rate is determined by the suitable formula in section 3.11.1.

Assuming that these general guidelines are followed, the reaction of the camera will be one of four cases, which are described in sections 3.3.4.1, 3.3.4.2, 3.3.4.3 and 3.3.4.4.

The FlashOut signal can be set into a mode where it is high while the effective exposure occurs, i.e. while the Integrate Enabled signal is high.

3.3.4.1 Free-run Mode with Asynchronous Timing

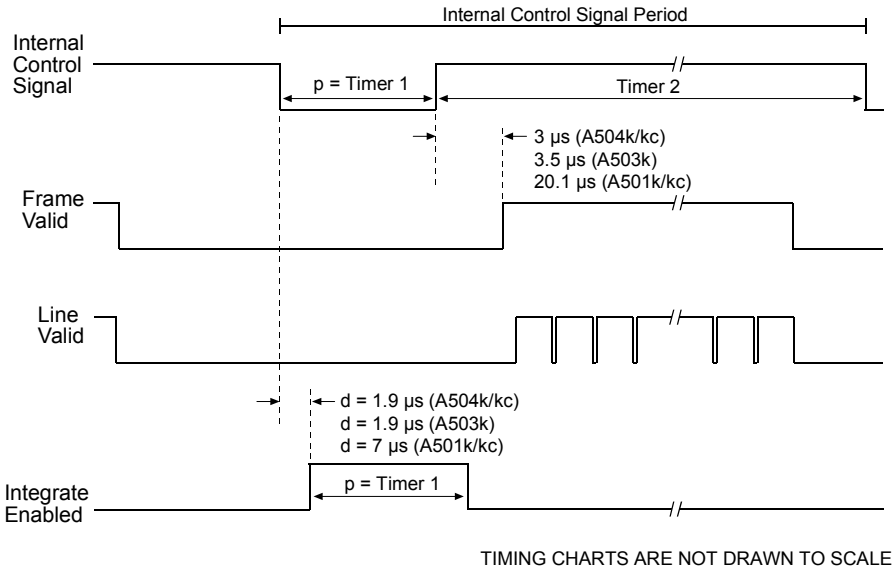


Figure 3-20: Free-run, Programmable Mode - Exposure Start and Stop with Frame Valid Low

The effective exposure starts and stops while the Frame Valid signal is low. The FlashOut signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-20):

- The effective exposure starts d microseconds after the rise of the internal control signal (exposure start delay).
- The duration of the effective exposure is defined by Timer 1.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by Timer 1		
d	1.9 µs	1.9 µs	7 µs

3.3.4.2 Free-run Mode with Synchronous/Asynchronous Timing

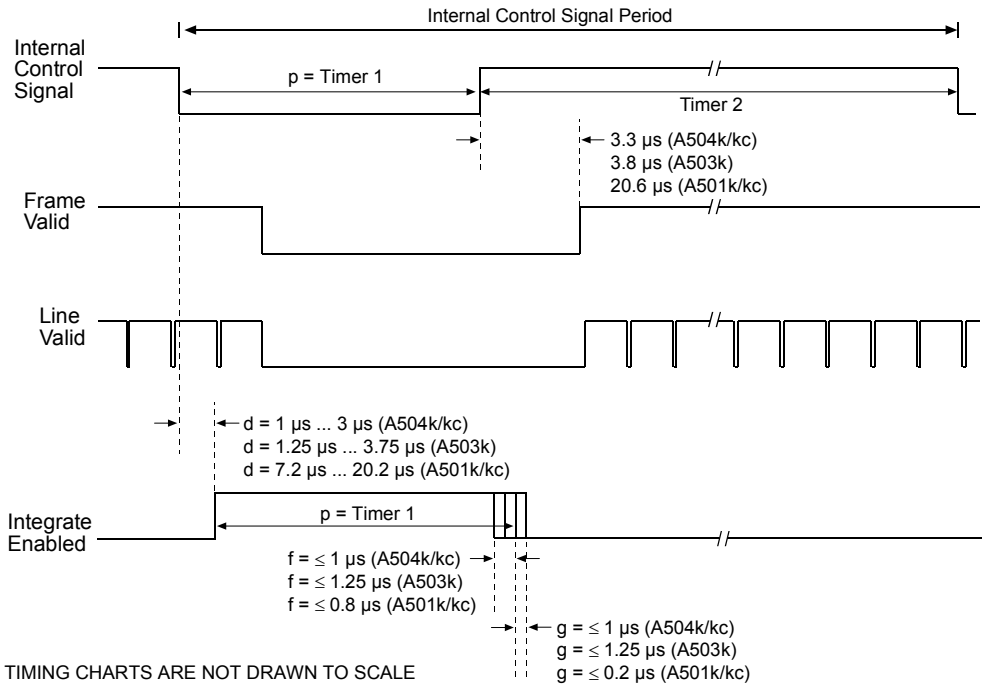


Figure 3-21: Free-run, Programmable Mode - Exposure Start with Frame Valid High, Exposure Stop with Frame Valid Low

The effective exposure starts while the Frame Valid signal is high and stops while the Frame Valid signal is low. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-21):

- The effective exposure starts d microseconds after the fall of the internal control signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter may shorten (f) or extend (g) the effective exposure, i.e. duration of the effective exposure = (p - f) to (p + g).

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by Timer 1		
d	1 µs ... 3 µs	1.25 µs ... 3.75 µs	7.2 µs ... 20.2 µs
f	< 1 µs	≤ 1.25 µs	< 0.8 µs
g	< 1 µs	≤ 1.25 µs	< 0.2 µs

3.3.4.3 Free-run Mode with Synchronous Timing 1

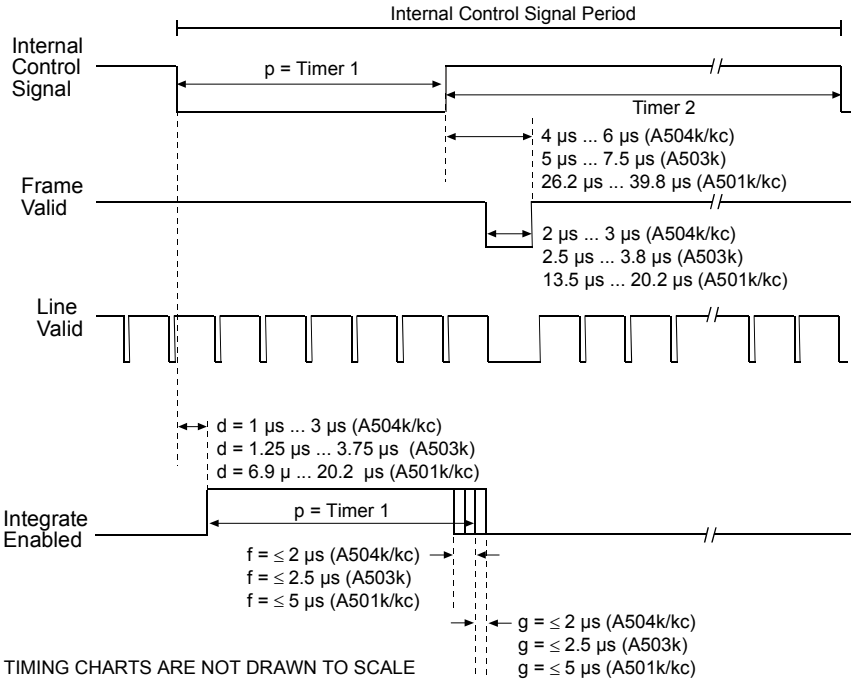


Figure 3-22: Free-run, Programmable Mode - Exposure Start and Stop with Frame Valid High

The effective exposure starts and stops while the Frame Valid signal is high. The Intergrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-22):

- The effective exposure starts d microseconds after the fall of the internal control signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter may shorten (f) or extend (g) the effective exposure, i.e.
  duration of the effective exposure = (p - f) to (p + g).
- The duration of the effective exposure can only occur in multiples of m microseconds.

	A504k/kc	**A503k**	**A501k/kc**
p	Exposure as set by Timer 1		
d	1 µs ... 3 µs	1.25 µs ... 3.75 µs	6.9 µs ... 20.2 µs
f	≤ 2 µs	≤ 2.5 µs	≤ 5 µs
g	≤ 2 µs	≤ 2.5 µs	≤ 5 µs
m	2 µs	2.5 µs	13.2 µs

3.3.4.4 Free-run Mode with Synchronous Timing 2

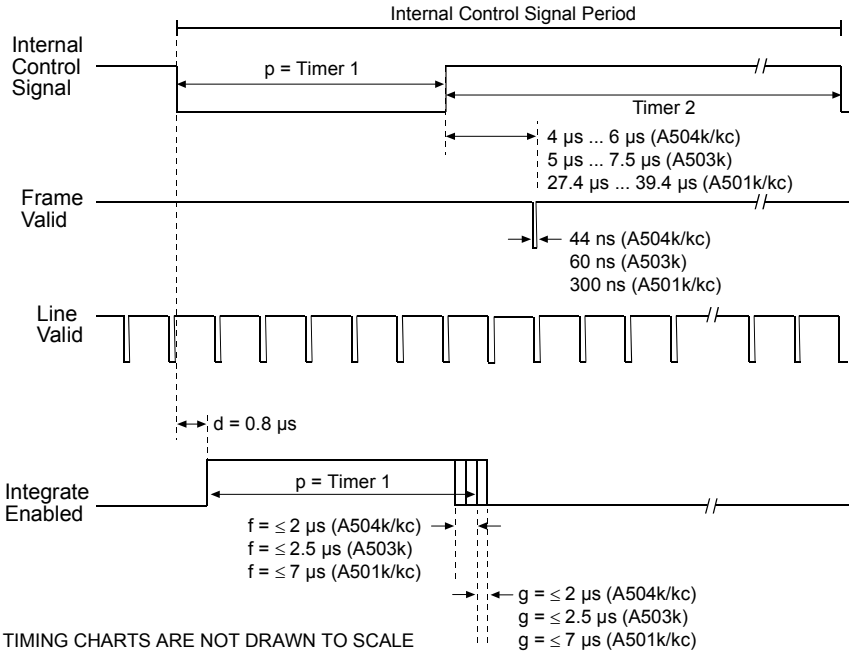


Figure 3-23:Free-run, Programmable Mode - Exposure Start and Stop with Frame Valid High

The effective exposure starts and stops while the Frame Valid signal is high. The Integrate Enabled signal is set to high while the effective exposure occurs. The start, stop, and duration of the effective exposure are defined in the following ways (see Figure 3-23):

- The effective exposure starts d microseconds after the fall of the internal control signal (exposure start delay).
- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter may shorten (f) or extend (g) the effective exposure, i.e.
  duration of the effective exposure = (p - f) to (p + g).
- The duration of the effective exposure can only occur in multiples of m microseconds.

	A504k/kc	**A503k**	**A501k/kc**
p	exposure set by Timer 1		
d	0.8 µs	0.8 µs	0.8 µs
f	≤ 2 µs	≤ 2.5 µs	≤ 7 µs
g	≤ 2 µs	≤ 2.5 µs	≤ 7 µs
m	2 µs	2.5 µs	13.2 µs

3.3.5 Free-run VGA Mode (A504k/kc Only)

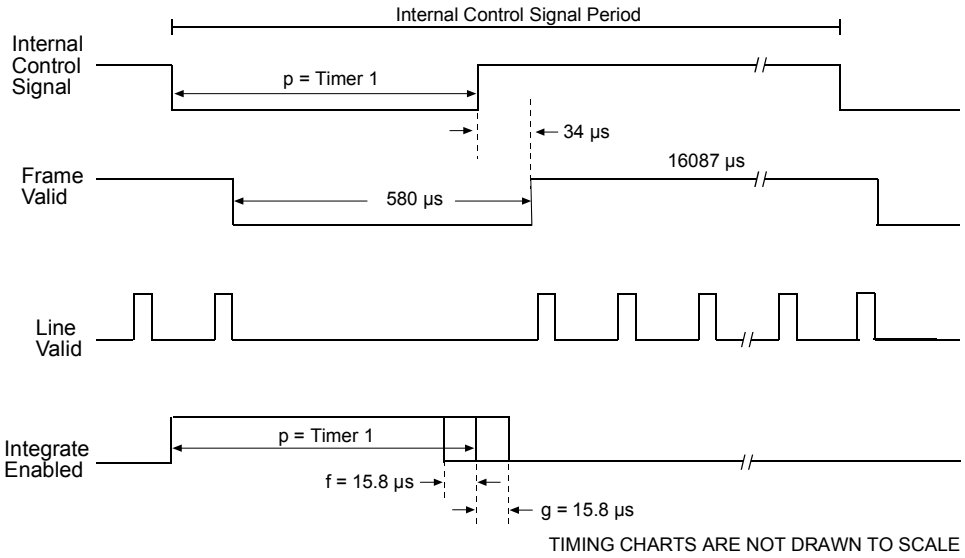


Figure 3-24: Free-run VGA Mode

- Disregarding possible jitter, the duration of the effective exposure is defined by period p (set by Timer 1).
- Jitter may shorten or extend the effective exposure, i.e. duration of the effective exposure = (p - 15.8 µs) to (p + 15.8 µs).
- The duration of the effective exposure can only occur in multiples of 15.8 µs microseconds.

	Timer 1 must be set to a minimum of 10 µs and to a maximum of 16645 µs. With very low exposures, use flash light.

3.4 Long Exposure Compensation (A504k/kc, A503k Only)

The long exposure compensation value can be set to optimize image quality. The longer the exposure time, the higher the long exposure compensation needs to be. The long exposure compensation value determines the reset voltage which is applied to the pixels between two images to achieve full and uniform discharge.

If the long exposure compensation is too low at a long exposure time, the image shows photo response non-uniformity (PRNU).

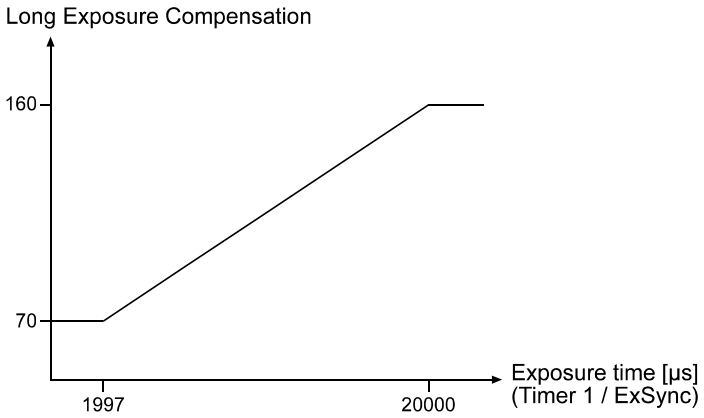


Figure 3-25: Long Exposure Compensation

If the long exposure compensation is too high at a short exposure time, the dynamic range and the sensitivity are reduced.

Set the long exposure compensation manually according to the following formula or according to Table 3-1:

$1997 \leq \text{exposure time} \leq 20000$: Long Exposure Compensation = (Timer 1 - 1997) x (90 / 18003) + 70
(rounded to the next integer value)

Exposure time* [µs]	Long exposure Commpensation
20000	160
15000	135
10000	110
8000	100
4000	80
2000	70

Timer 1 determines the exposure time in programmable and free-run mode. The exposure time is determined by ExSync in edge-controlled and level-controlled mode.

Table 3-1: Long Exposure Compensation Sample Values

You can set long exposure compensation using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2).

3.5 Max Exposure Time at Max Speed (A504k/kc Only)

In many applications, cameras are operated at maximum speed and at maximum exposure time. To obtain a reliable timing for frame read-out in synchronous timing 2, follow the setup recommendations described in this section. This recommendation applies to level-controlled, programmable, free-run VGA and free-run, programmable exposure time control modes. It is not relevant for edge-controlled mode.

In free-run mode, the frame rate is equal to 1 divided by (Timer 1 plus Timer 2). In other modes, the frame rate is equal to 1 divided by (ExSync high time plus ExSync low time).

For maximum exposure, Timer 2 must always be set to 3 µs in free-run and programmable mode. In level-controlled mode, the ExSync high time must always be set to 5 µs.

With these values, the exposure time can be calculated. To achieve a reliable synchronous timing 2 at full frame rate, however, we recommend that you use the **calculated exposure time minus 1 µs**.

Example for free-run mode

The aim is to achieve the maximum exposure time possible with a frame rate of 500 fps at full AOI.

$$\text{Timer 1} = \frac{1}{\text{frame rate}} - \text{Timer 2} - 1\ \mu s$$

$$\text{Timer 1} = \frac{1}{500} - 3\ \mu s - 1\ \mu s$$

To achieve the maximum exposure time with a frame rate of 500 fps at full AOI, Timer 1 must be set to 1996 µs.

Table 3-2 shows the maximum recommended Timer 1 and ExSync low time values for different maximum frame rates at different AOI Height values. Timer 2 is assumed to be 3 µs, the ExSync high time 5 µs.

Max. Frames Per Second	AOI Height	Timer 1 [µs] Programmable, Free-run	ExSync Low Time [µs] Level-controlled
500	1024	1996	1994
1000	512	996	994
2000	256	496	494
4000	128	246	244
8000	64	121	119
16000	32	58	56

Table 3-2: Recommended Max Exposure Time at Max Speed

3.6 Color Creation in the A504kc and A501kc

The CMOS sensor used in the color version of the camera is equipped with an additive color separation filter. With the color filter, each individual pixel is covered by a micro-lens which allows light of only one color to strike the pixel. The pattern of the color filter is shown in Figure 3-26. As the figure illustrates, in each block of four pixels, one pixel is struck by red light, one is struck by blue light and two pixels are struck by green light.

The pattern used in the **A504kc** and the **A501kc** is that of the Bayer Filter. The first line starts with GR.

Since each individual pixel gathers information on only one color, an interpolation must be made from the surrounding pixels to get full RGB data for the pixel. A DLL that can be used to convert the output from the color camera into RGB color information is available through Basler support.

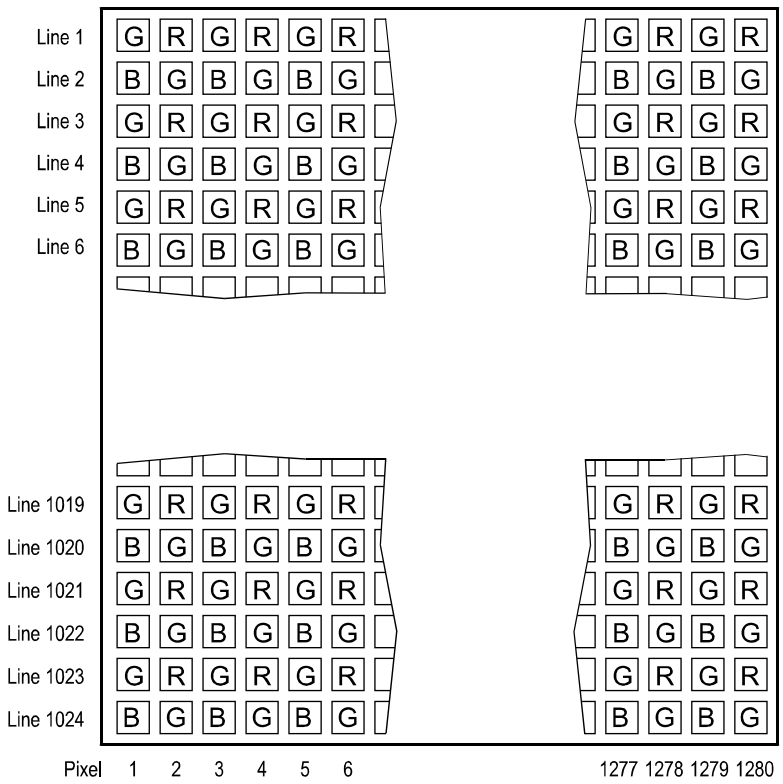


Figure 3-26: Bayer Filter Pattern

IR Cut Filter

In applications using the normal range of visible light we recommend that you place an IR cut filter in front of your F-mount lens.

3.7 Gain and Offset

The **A500k** includes a CMOS sensor with 1024 ADCs (Analog to Digital Converters), and a digital shifter.

The pixels in the CMOS sensor output voltage signals when they are exposed to light. After readout of the pixel voltage, an offset is added to each voltage. The voltages are then transferred to the ADCs which convert the voltages to digital output signals. The ADC reference is used to set the gain, but only in a small range. The 10 bit data from the ADCs in the sensor enters the digital shifter in the camera electronics where the 8 bits to be output are selected from the 10 bits output by the sensor.

As shown in Figures 3-27 and 3-28, the gain is increased or decreased by decreasing or increasing the ADC reference. Increasing or decreasing the offset moves the input signal up or down the measurement scale but does not change the signal amplitude.

For most applications, black should have a gray value of 1 and white should have a gray value of 254. Attempt to achieve this by varying exposure and illumination rather than changing the camera's gain. The default gain (gain register = 98) is the optimal operating point (minimum noise) and should be used if possible.

The gain can either be changed via the corresponding ADC reference which can be set in the gain register, or by selecting different bits in the digital shifter.

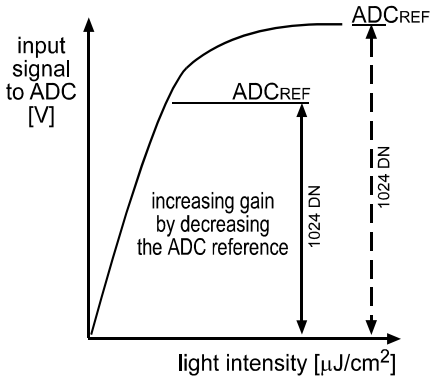


Figure 3-27: Gain

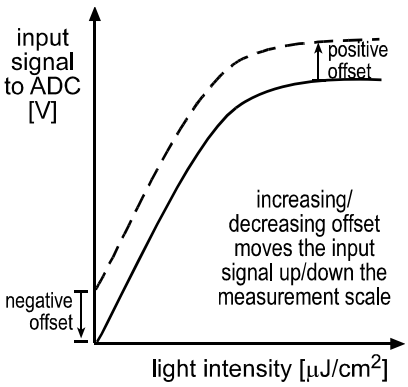


Figure 3-28: Offset

ⓘ	Raising the gain via the ADC reference has the consequence that noise is increased so that the signal-to-noise ratio decreases. In addition, missing codes may degrade the image quality severely. We recommend that you do not change the gain via the ADC reference. The default gain register setting is 98.

In order to obtain a higher gain factor of up to 8, use the digital shift in combination with the gain register (for an explanation of the digital shifter, see section 3.10.).

You can set the gain and offset using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2).

3.7.1 Gain Settings in More Detail

The optical gain Gopt is the digital number value (DN) that the camera outputs after an exposure with the amount of light of 1 Lux per second. For this camera, the optical gain can be calculated as follows (formula based on data from sensor data sheet):

$$Gopt = \frac{1.6 \text{ DN / lx s}}{0.006 - 0.0000203125 \times Gain}$$

If you know the optical amplification you want to achieve, and need to know the Gain register setting, use the following formula (data based on sensor data sheet):

$$\text{Gain register} = 295.38 - \frac{1.6 \text{ DN / lx s}}{0.0000203125 \times Gopt}$$

Some sample values calculated with these formula are listed below:

- If the Gain register is set to **98 (recommended)**, the optical gain Gopt is 400 DN / lx s (if digital shift = 0). Gopt can vary slightly between different cameras.
- If the Gain register is set to 196, the optical gain Gopt is 800 DN / lx s (if digital shift = 0). Gopt can vary between different cameras. The value corresponds to a gain factor of two compared to the gain achieved with a gain register setting of 98. This is the maximum gain we recommend.

Note that the calculated values are typical values which can vary slightly between different cameras.

If the gain you selected is too high, the image will show pixelwise/columnwise missing codes. We recommend that you do not use gain register values higher than **196**. If youwish to increase the gain further, select the next higher digital shift value and reset the gain register value to 98.

If the gain you selected is too low, the image will show pixel saturation.

With a digital shift of 1, the optical gain must be multiplied by 2. With a digital shift of 2, the optical gain must be multiplied by 4. See section 3.10.

3.7.2 Offset Settings in More Detail

The offset can be trimmed in two directions by using either the OfsPos register (see section 4.2.4.7) that moves the offset up, or by using the OfsNeg register (see section 4.2.4.6) that moves the offset down. If you move the offset down, set the OfsPos register to 0. If you move the offset up, set the OfsNeg register to 0.

3.8 DSNU Constancy (A503k Only)

In theory, when an area scan camera with a digital sensor captures a frame in complete darkness, all of the pixel values in the frame should be near zero and they should be equal. In practice, slight variations in the performance of the pixels in the sensor will cause some variation in the pixel values output from the camera. This variation is known as Dark Signal Non-uniformity (DSNU). In addition, the DSNU associated with non-overlapped exposure differs from the DSNU associated with overlapped exposure.

With the DSNU constancy feature enabled, the DSNU associated with non-overlaped exposure will be replaced and the DSNU associated with overlapped exposure will apply to both non-overlapped and overlapped exposure. Accordingly, the unwanted difference in the DSNUs will not become apparent when non-overlapped and overlapped exposure are used in an alternating fashion.

To prevent a decrease of image quality we do not recommend enabling the DSNU constancy feature when operating the camera at frame rates of < 30 fps.

You can enable and disable the DSNU constancy feature using either the Camera Configuration Tool Plus (see section 4.1) or binary commands from within your application to set the camera's DSNU Constancy and Shutterline Correction Enable register (see section 4.2).

See section 4.2.4.8 for more information on the DSNU Constancy and Shutterline Correction Enable register.

3.9 Shutterline Correction (A503k Only)

When the camera operates with overlapped exposure, frame N is still being read out when the exposure of frame N+1 is triggered.

The shutterline of frame N is the line that is being read out when the exposure of frame N+1 is triggered. The trigger, however, causes a fluctuation of voltage leading to a decrease of the pixel values in the shutterline.

With the shutterline correction feature enabled, a value is added to the pixel values to compensate for the effect of the voltage fluctuation. The value to be added can be set using the Shutterline Correction register.

You can enable and disable the shutterline correction feature and set a value using either the Camera Configuration Tool Plus (see section 4.1) or binary commands from within your application to set the camera's DSNU Constancy and Shutterline Correction Enable register and the Shutterline Correction register (see section 4.2).

See section 4.2.4.8 for more information on the DSNU Constancy and Shutterline Correction Enable register. See section 4.2.4.9 for more information on the Shutterline Correction register.

3.10 Digital Shift

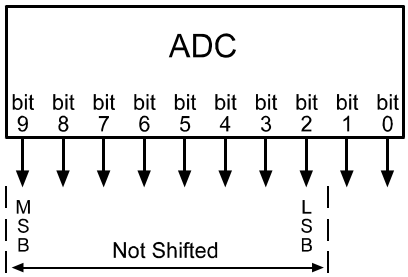
The digital shift feature allows you to change the group of bits that is output from the ADC. Using the digital shift feature will effectively multiply the output of the CMOS sensor by 2 times, 4 times or 8 times. Section 3.10.1 describes how digital shift works.

You can set digital shift using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2).

3.10.1 How Digital Shift Works

No Shift

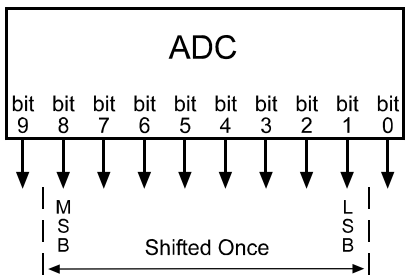
As mentioned in section 3.1, the **A500k** uses 10 bit ADCs to digitize the output from the CMOS sensor. The camera drops the least two significant bits from the ADC and transmits the 8 most significant bits (bit 9 through bit 2).



Shift Once

When the camera is set to shift once, the output from the camera will include bit 8 through bit 1 from the ADC.

The result of shifting once is that the output of the camera is effectively doubled. For example, assume that the camera is set for no shift, that it is viewing a uniform white target and that under these conditions the reading for the brightest pixel is 20. If we changed the digital shift setting to shift once, the reading would increase to 40.

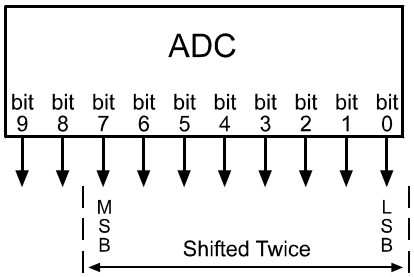


	Note that if bit 9 is set to 1, all of the other bits will automatically be set to 1. This means that you should only use the shift once setting when your pixel readings with no digital shift are all below 128.

Shift Twice

When the camera is set to shift twice, the output from the camera will include bit 7 through bit 0 from the ADC.

The result of shifting twice is that the output of the camera is effectively multiplied by four. For example, assume that the camera is set for no shift, that it is viewing a uniform white target, and that under these conditions the reading for the brightest pixel is 20. If we changed the digital shift setting to shift twice, the reading would increase to 80.

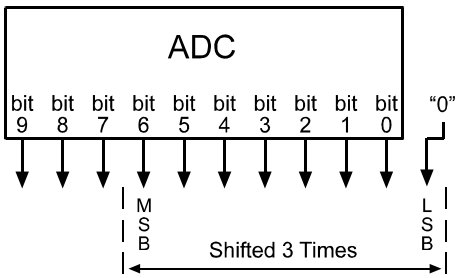


	Note that if bit 9 or bit 8 is set to 1, all of the other bits will automatically be set to 1. This means that you should only use the shift twice setting when your pixel readings with no digital shift are all below 64.

Shift Three Times

When the camera is set to shift three times, the output from the camera will include bit 6 through bit 0 from each ADC along with a zero as the LSB.

The result of shifting three times is that the output of the camera is effectively multiplied by eight. For example, assume that the camera is set for no shift, that it is viewing a uniform white target and that under these conditions the reading for the brightest pixel is 20. If you changed the digital shift setting to shift three times, the reading would increase to 160.



	Note that if bit 9, bit 8 or bit 7 is set to 1, all of the other bits will automatically be set to 1. This means that you should only use the shift three times setting when your pixel readings with no digital shift are all below 32. Since the shift three times setting requires that the least significant bit always be 0, no odd gray values can be output. In this case, the gray value scale will only include gray values of two, four, six and so forth.

3.10.2 Precautions When Using Digital Shift

There are several checks and precautions that you must follow before using the digital shift feature.

Make this check:

1. Use the binary commands or the CCT+ to set the camera for no digital shift.
2. Check the output of the camera under your normal lighting conditions with no digital shift and note the readings for the brightest pixels.
   - If any of the readings are above 128, do not use digital shift.
   - If all of the readings are below 128, you can safely use the 2X digital shift setting.
   - If all of the readings are below 64, you can safely use the 2X or 4X digital shift setting.

3.11 Area of Interest (AOI)

The area of interest feature allows you to specify a portion of the CMOS array and during operation, only the pixel information from the specified portion is transferred out of the camera.

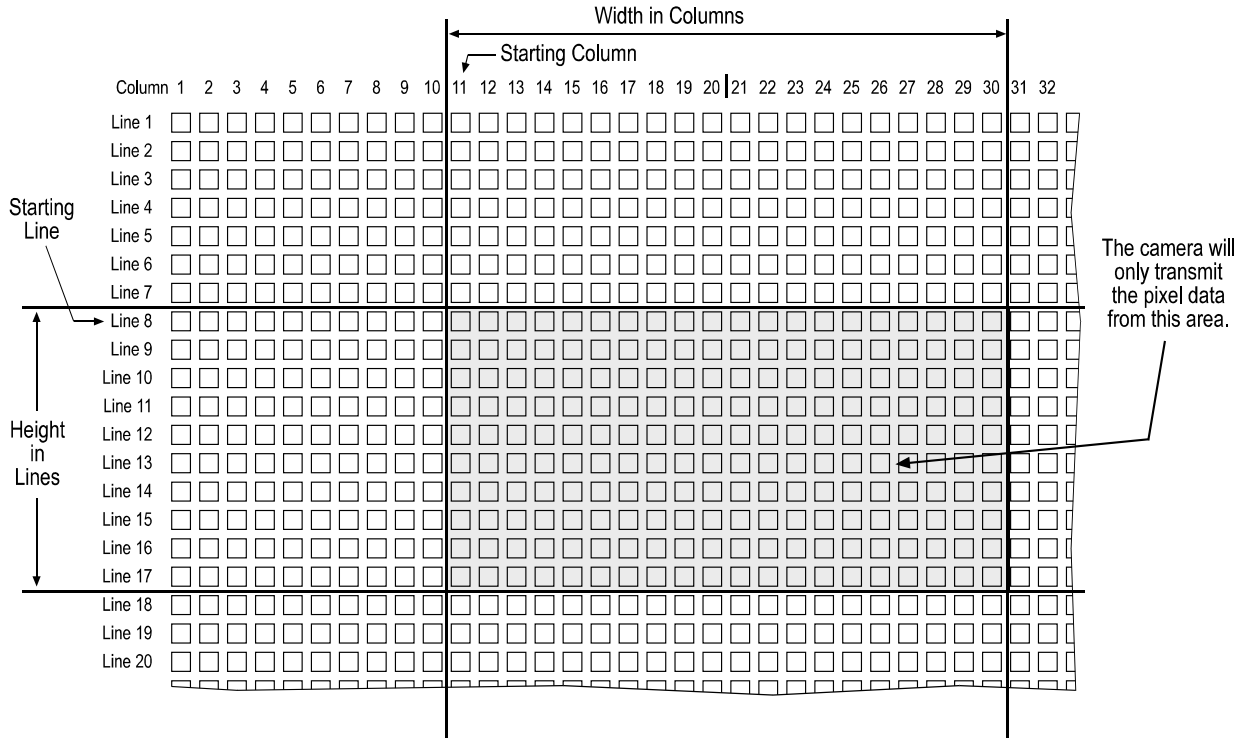
The size of the area of interest is defined by declaring a starting column, a width in columns, a starting line and a height in lines.

Starting columns can only be chosen in multiples of 10 + 1 due to the way the data is output of the sensor (see Figure 3-1).

Widths can only be chosen in multiples of 10 (**A504k/kc**, **A501k/kc**) or 40 (**A503k**) due to the way the data is output of the sensor.

For example (applicable to **A504k/kc**, **A501k/kc**), suppose that you specify the starting column as 11, the width in columns as 20, the starting line as 8 and the height in lines as 10. As shown in Figure 3-29, the camera will only transmit pixel data from within the defined area.

Information from the pixels outside of the area of interest is discarded.



Due to the video output, starting columns can only be selected in multiples of 10 + 1, i.e. only columns 1, 11, 21 and so on can be selected.

Figure 3-29: Area of Interest (Example for **A504k/kc**, **A501k/kc**)

You can set the area of interest using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2). You use the Area of Interest Starting Column, Area of Interest Width in Columns, Area of Interest Starting Line and Area of Interest Height in Lines commands.

	Note that the binary commands start to count at 0.

	In normal operation, the camera is set to use all of the pixels in the array. To use all of the pixels, the starting column should be set to 1, the width in columns to 1280, the starting line to 1 and the height in lines to 1024. The setting for the width in lines and for the starting column must be divisible by 10. The minimum width is 10. The minimum height in lines is 2. The minimum starting line is 0. The sum of the setting for the starting column plus the setting for the width in columns can not exceed 1281. The sum of the setting for the starting line plus the setting for the height in lines can not exceed 1025. For a color camera, the setting for the height in lines and for the starting line must be divisible by two. The minimum height in lines is 2.

3.11.1 Changes to the Maximum Frame Rate with Area of Interest

When the area of interest feature is used, the camera's maximum achieveable frame rate increases. The amount that the maximum frame rate increases depends on the number of lines included in the area of interest (AOI height). The fewer the number of lines in the area of interest, the higher the maximum frame rate. The maximum achieveable frame rate can be calculated using the following formula:

A504k/kc:

$$\text{Maximum frames per second (approximated)} = \frac{67580000\ [s^{-1}]}{\text{AOI Height} \times 132}$$

A503k:

$$\text{Max. frames per second (approx.)} = \frac{67580000\ [s^{-1}]}{\text{AOI Height} \times 164}$$

for AOI Width = 1280 (full width)

$$\text{Max. frames per second (approx.)} = \frac{67580000\ [s^{-1}]}{\text{AOI Height} \times \left(4 + \frac{\text{AOI Width}}{8}\right)}$$

for $1040 \leq \text{AOI Width} < 1280$

:

$$\text{Max. frames per second (approx.)} = \frac{67580000\ [s^{-1}]}{\text{AOI Height} \times 132}$$

for $\text{AOI Width} < 1040$

A501k/kc:

$$\text{Max. frames per second (approx.)} = \frac{100\ \text{MHz}}{1320 \times (\text{AOI Height} + 1)}$$

3.11.2 Dynamic Area of Interest (A504k/kc, A503k Only)

Dynamic AOI is a useful feature for object tracking applications. It needs to be activated if you want to displace the AOI position diagonally.

To show the usefulness of this feature, this section explains first what happens if you move the AOI diagonally with Dynamic AOI deactivated. When you change the AOI starting line register, the value becomes immediately active. As a result, the AOI shifts vertically in one of the next images. Since you can only write commands to the camera sequentially, you would enter the AOI starting column register next. The value becomes active and the AOI shifts horizontally in one of the next images. Even if the commands are written immediately after one another, the image output is so fast that the commands will be realized separately in different images. With Dynamic AOI deactivated, shifting the AOI position diagonally can only be achieved via an intermediate AOI position.

With Dynamic AOI activated, the AOI shifts diagonally without moving to an intermediate position. You enter the AOI values as follows:

1. You write the AOI Starting Line register. It does not yet become active.
2. You write the AOI Starting Column register.

   Now both values become active in the camera at the same time.

AOI Width and AOI Height are not affected by dynamic AOI.

With Dynamic AOI, the AOI can only shift in steps of 10 columns and 10 lines due to the limitations for choosing AOI starting columns (see section 3.11).

You can activate or deactivate Dynamic AOI using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2.4.15 ”Area of Interest Stamp and Dynamic Area of Interest (A504k/kc, A503k Only)”).

3.11.3 Area of Interest Stamp (A504k/kc, A503k Only)

A command sent to the camera will become active only after a short latency. At low frame rates, the command usually becomes active for the next image. At high frame rates you do not know on exactly which image the command will become active. This information is especially required for tracking applications where the camera is operating at a high frame rate and the area of interest is changed frequently. Information about the selected AOI can be stamped into the image.

If the area of interest stamp feature is activated, the stamp is applied to the last 10 pixels of the last line, that is, the bottom right of every image. It replaces the image information for these pixels (1 Byte per pixel). The stamp contains the following information:

Pixel0 high byte	Pixel1 low byte	Pixel2 high byte	Pixel3 low byte	Pixel4 high byte	Pixel5 low byte	Pixel6 high byte	Pixel7 low byte	Pixel8 high byte	Pixel9 low byte
Frame Counter		AOI Starting Column		AOI Width		AOI Starting Line		AOI Height	

Table 3-3: AOI Stamp Structure

Frame Counter: 16 Bit counter. The counter is increased by one with each image and ranges from 0 to 65535. After 65535, the counter restarts at 0. The counter can not be reset.

AOI Starting Column, AOI Width, AOI Starting Line, AOI Height: The values come directly from the AOI registers of the camera. The AOI values are located right-justified in each 16 Bit stamp. Unused Bits are set to 0.

	The stamp is not applied • if a test image is active, or • if the exposure mode is set to free-run, VGA.

You can activate or deactivate the Area of Interest Stamp using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2.4.15 "Area of Interest Stamp and Dynamic Area of Interest (A504k/kc, A503k Only)").

3.11.4 Area of Interest with the VGA Monitor Output (A504k/kc Only)

	In VGA exposure mode, the maximum frame rate remains 60 fps (frames per second), regardless of the area of interest selected.

In the VGA exposure mode, 1280 x 960 pixels of the image are scaled down to 640 x 480 pixels. These always transferred via the VGA monitor output, even if a smaller area of interest is selected. If an area of interest is set, the pixels inside the area of interest display an image. The pixels outside the area of interest are black.

Via the Camera Link output, only the pixels inside the area of interest are transferred.

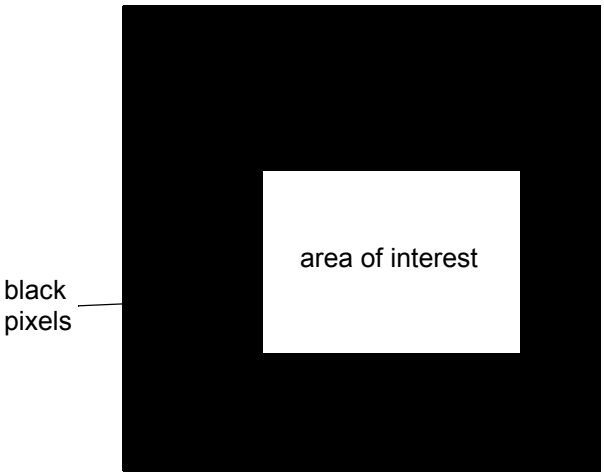


Figure 3-30: Area of Interest with VGA Monitor Output

3.12 Test Images

The test image mode is used to check the camera's basic functionality and its ability to transmit an image via the video data cable. The test image can be used for service purposes and for failure diagnostics. In test mode, the image is generated with a software program and the camera's digital devices and does not use the optics, CMOS sensor, or ADCs.

You can put the camera in test image mode using either the Camera Configuration Tool Plus (see section 4.1) or binary commands (see section 4.2). You use Test Image command.

When one of the test images is active, the gain, offset and exposure time have no effect on the image.

There are four test images:

- a gray scale test image
- a color test image (**A504kc** and **A501kc** only)
- a running line test image
- a white screen test image

If the camera is set for an exposure mode that uses an ExSync signal, an ExSync signal is required to output the test image. If the camera is set for free-run, each cycle of the camera's internal sync signal will trigger the output of a test image.

3.12.1 Gray Scale Test Image

The gray scale test image consists of lines with repeated gray scale gradients ranging from 0 to 255. The first line starts with a gray value of 0 on the first pixel, in the second line the first pixel has a gray value of 1, in the third line the first pixel has a gray value of 2, and so on.

The mathematical expression for the test image is: gray level = [x + y] MOD 256. This expression is shown graphically in Figure 3-32.

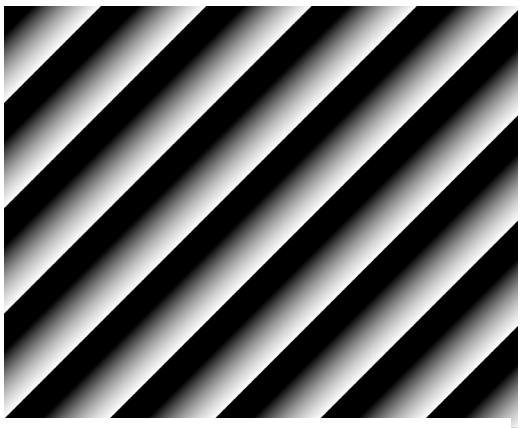


Figure 3-31: Test Image

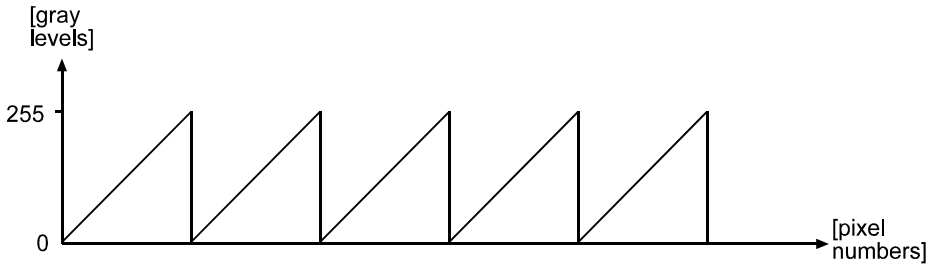


Figure 3-32: Formation of the Monochrome Test Image

3.12.2 Color Test Image (A504kc and A501kc Only)

The color test image is similar to the gray scale test image, except that the first gray scale stripe is red, the second green, the third blue, the fourth white, the fifth red again.

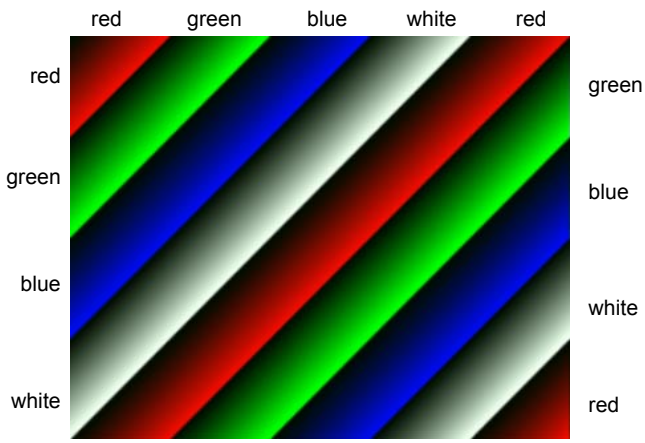


Figure 3-33: Test Image

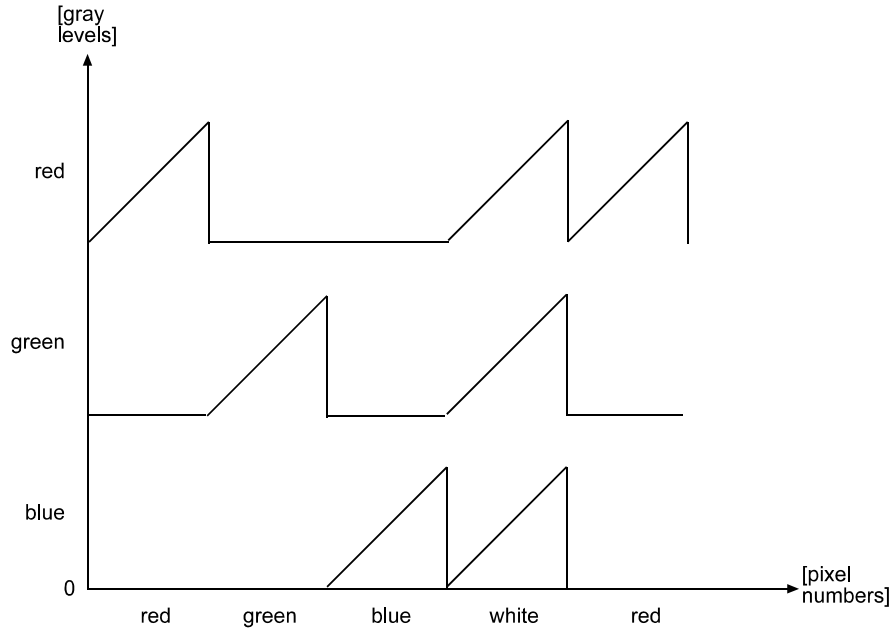


Figure 3-34: Formation of the Color Test Image; the First Line is Shown

The color test image is only displayed correctly if the pixels are sorted according to the color pattern described in section 3.6.

3.12.3 Running Line Test Image

This test image mode tests frame capture. A black image has a white line with a height of one pixel. This horizontal line moves down by one pixel after each frame.

Figure 3-35: Test Image

3.12.4 White Screen Test Image

This test image mode outputs a white screen.

3.13 Configuration Sets

The camera's adjustable parameters are stored in configuration sets and each configuration set contains all of the parameters needed to control the camera. There are three different types of configuration sets: the Work Set, the Factory Set and User Sets.

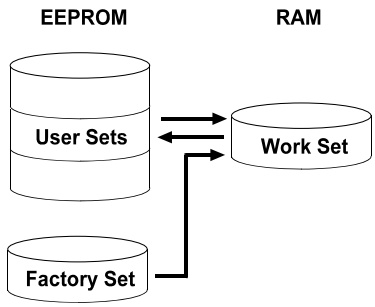


Figure 3-36: Config Sets

Work Set

The Work Set contains the current camera settings and thus determines the camera's present performance, that is, what your image currently looks like. The Work Set is stored in the camera RAM. The configuration parameters in the Work Set can be altered directly using the Camera Configuration Tool Plus or using binary programming commands.

Factory Set

When a camera is manufactured, a test set up is performed on the camera and an optimized configuration is determined. The Factory Set contains the camera's factory optimized configuration. The Factory Set is stored in non-volatile memory on the EEPROM and can not be altered.

User Sets

User Sets are also stored in the non-volatile EEPROM of the camera. The camera has 15 User Sets. Each User Set initially contains factory settings but User Sets can be modified. Modification is accomplished by making changes to the Work Set and then copying the Work set into one of the User Sets. The Camera Configuration Tool Plus or binary commands can be used to copy the Work Set into one of the User Sets.

Startup Pointer

When power to the camera is switched off, the Work set in the RAM is lost. At the next power on, a configuration set is automatically copied into the Work Set. The Startup Pointer is used to specify which of the configuration sets stored in the EEPROM will be copied into the Work Set at power on. The Startup Pointer is initially set so that the Factory Set is loaded into the Work Set at power on. This can be changed using the Camera Configuration Tool Plus or binary commands. The Startup Pointer can be set to the Factory Set or to any one of the User Sets. So, for example, if the Startup Pointer is set to User Set 13, then User Set 13 will be copied into the Work Set at Power on.

You can work with configuration sets and the startup pointer using either the CCT+ (see section 4.1 and the configuration tool's on-line help file) or binary commands (see section 4.2).

With the CCT+, you can use the Camera menu to copy the Work Set to a User Set, to Copy a User Set or the Factory Set to the Work Set, or to set the Startup Pointer.

With binary commands you use the Copy Work Set to User Set command, the Copy Factory Set or User Set to Work Set command, and the Select Startup Pointer command to manipulate configuration sets.

3.14 Camera Status

A500k cameras monitor their status by performing a regular series of self checks. The current status of a camera can be viewed in several ways:

- with the camera configuration tool CCT+. You can use the Camera Status information in the Camera Information group (see section 4.1 and the configuration tool's on-line help).
- with binary commands (see section 4.2). You can use the Camera Status command to see if the camera has detected any errors.
- by checking the LED on the back of the camera. If certain error conditions are present, the LED will flash (see section 6.1.1).

4 Configuring the Camera

A500k cameras come factory-set so that they will work properly for most applications with minor changes to the camera configuration. For normal operation, the following parameters are usually configured by the user:

- Exposure time control mode
- Exposure time (for ExSync programmable mode or free-run programmable mode)
- Long Exposure Compensation (**A504k/kc, A503k** only)

To customize operation for your particular application, the following parameters can also be configured:

- Gain
- Offset
- DSNU Constancy and Shutterline Correction (**A503k** only)
- Digital Shift
- Area of Interest
- Dynamic Area of Interest
- Area of Interest Stamp
- Flash Trigger

The camera is programmable via the serial port. Two methods can be used to change the camera's settings. The first and easier approach is to change the settings using the Camera Configuration Tool Plus (CCT+). See section 4.1 for complete instructions on using the configuration tool. You can also change the settings directly from your application using binary commands. Section 4.2 lists the commands and provides instructions for their use.

4.1 Configuring the Camera with the Camera Configuration Tool Plus (CCT+)

The camera configuration tool CCT+ is a Windows™ based program used to easily change the camera's settings. The tool communicates via the RS-644 serial connection in the Camera Link interface between the frame grabber and the camera. The tool automatically generates the binary programming commands that are described in section 4.2. For instructions on installing the tool, see the installation booklet that was shipped with the camera.

This manual assumes that you are familiar with Microsoft Windows and that you have a basic knowledge of how to use programs. Otherwise, refer to your Microsoft Windows manual.

4.1.1 Opening the Configuration Tool

1. Make sure that the properties for the RS-644 serial port on your frame grabber are properly configured and that the camera has power.
2. To start the CCT+, click **Start**, click **Basler Vision Technologies**, and then click **CCT+** (default installation).

   During start-up, a start-up screen can be seen.

   If start-up is successful, the tool will open. To familiarize yourself with using the tool, press the **F1** key and look through the online help included with the tool.

   If an error occurs, the tool is automatically closed after start-up. Refer to the CCT+ Installation Guide for possible causes.

4.1.2 Closing the Configuration Tool

Close the CCT+ by clicking on the ☒ button in the upper right corner of the window.

4.1.3 Configuration Tool Basics

The RAM memory in the camera contains the set of parameters that controls the current operation of the camera. This set of parameters is known as the Work Set (see section 3.13). The CCT+ is used to view the present settings for the parameters in the Work Set or to change the settings.

When the CCT+ is opened and a port is selected, it queries the camera and displays a list of the current settings for the parameters in the Work Set.

To simplify navigation, parameters are organized in related groups. For example, all parameters related to the camera output can be found in the Output group.

When you click on the plus or minus sign beside a group (+ or -), the parameters in this group will be shown or hidden, respectively.

To get an overview of all parameters available on the connected camera, maximize the CCT+ window and click the + sign beside each group.

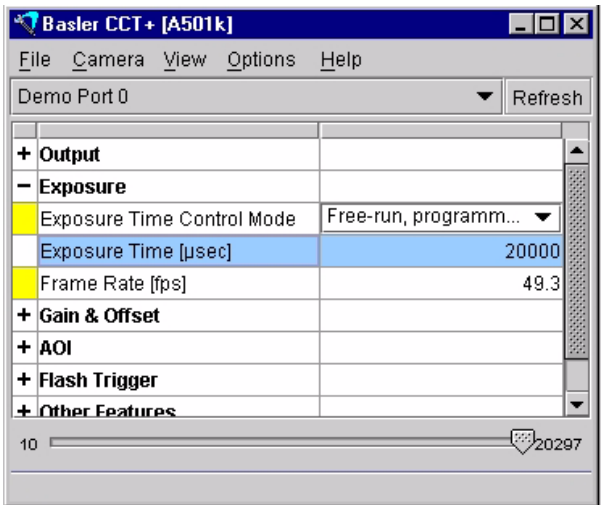


Figure 4-1: Exposure Group

The camera parameter names always appear in the left column of the list. The current setting for each parameter appears in the right column.

By default, a **Parameter Description** window is displayed. In this window, you can find basic information on the selected parameter and if present, on the dependencies that may exist between the selected parameter and other parameter(s).

If you make a change to one of the settings, that change will instantly be transmitted from the CCT+ to the camera's Work Set. Because the parameters in the Work Set control the current operation of the camera, you will see an immediate change in the camera's operation.

By default, the CCT+ automatically updates the displayed settings every 5 seconds. The feature behind this behavior is called Auto Refresh. If **Auto Refresh** is not enabled, the display will not update when a camera setting is changed using another tool, when power to the camera is switched off and on, or when the connected camera is exchanged while the CCT+ is displaying the camera settings. To manually refresh the display, you can use the **Refresh** button in the top right corner of the tool.

Keep in mind that the Work Set is stored in a volatile memory. Any changes you make to the Work Set using the configuration tool will be lost when the camera is switched off. To save changes you make to the Work Set, save the modified Work Set into one of the camera's 15 User Sets. The User Sets are stored in non-volatile memory and will not be lost when the camera is switched off (see section 3.13).

Alternatively, you can also save the Work Set to the hard disk of your computer and load it from hard disk.

If you want your changes to be loaded into the Work Set at the next power on, set the Startup Pointer to the User Set where you saved your changes.

4.1.4 Configuration Tool Help

The CCT+ includes a complete on-line help file which explains how to change a setting or to copy the Work Set to a User Set, to Copy a User Set or the Factory Set to the Work Set, or to set the Startup Pointer. To access on-line help, press the F1 key whenever the configuration tool is active.

4.2 Configuring the Camera with Binary Programming Commands

Configuration commands can be issued to the **A500k** via the RS-644 serial connection in the Camera Link interface between the frame grabber and the camera. Commands are issued using a binary protocol. With this protocol, data is placed into a frame and sent to the camera. Once the data is received it is checked for validity. If valid, the data is extracted and the command is executed.

If the command issued to the camera was a read command, the camera will respond by placing the requested data into a frame and sending it to the host computer.

A standard application programmer's interface (API) for asynchronous serial reading and writing via the RS-644 port on the frame grabber has been defined in the Camera Link standard (Appendix B, API Functions). All Camera Link compatible frame grabbers provide a software library (.dll file) named clser***.dll where *** is specific to the frame grabber vendor. There are four functions within that DLL:

- lSerialInit - Initialize the serial communication for a specific board.
- clSerialRead - Read bytes from the camera.
- clSerialWrite - Write bytes to the camera.
- clSerialClose - Close the serial communication.

To execute the binary programming commands, you can load the DLL for the frame grabber you are using into your programming tool. You can use either the API from the DLL delivered with the grabber or the Basler CPA driver for executing the binary commands.

The Basler CPA (Camera Port Access) is a software framework which standardizes access to the camera ports via frame grabbers from different vendors. With the help of the Basler CPA driver, you can read and write blocks of data to and from the camera. The binary command protocol is fully implemented in the CPA driver.

The CPA driver and a Programmer's Guide for the driver are both part of Basler's Classic Camera Configuration Tool. The Classic Camera Configuration Tool can be downloaded from the Basler website at: www.baslerweb.com/indizes/beitrag_index_en_71680.html.

The Basler Camera Configuration Tool is available in two versions: the Classic Camera Configuration Tool (Classic CCT) and the Camera Configuration Tool Plus (CCT+). The CPA driver and its Programmer's Guide are only included with the Classic CCT.

The **A500k** will only work with the CCT+ version of the configuration tool. If you want to use the configuration tool with an **A500k**, you must download and install the CCT+ version and you must use the CCT+ to access the camera.

If you would also like to use the CPA driver, you should download and install the Classic CCT. Once the Classic CCT is installed, you should check the path `C:\Program Files\Basler\Camera Config Tool\Cpa`. The Cpa folder will contain the files you need to work with the driver.

If you are using your camera with an optional Basler Interface Converter (k-BIC), you can configure the camera via the RS-232 serial connection between your PC and the k-BIC. The k-BIC is only available for the **A501k/kc**.

4.2.1 Command Frame and Response Format

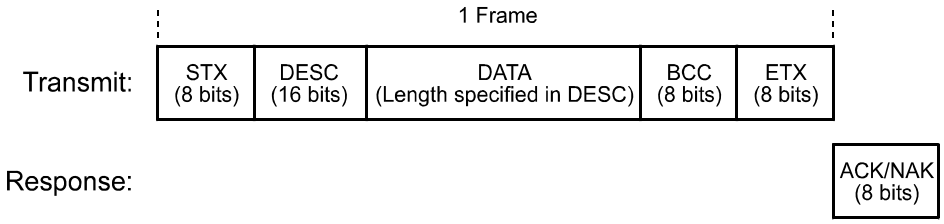


Figure 4-2: Representation of a Command Frame and Response

STX Identifies the start of the frame text
Size = 1 Byte
(The value of the STX byte is always 0x02)

DESC Descriptor
Size = 2 Bytes
The bits in the descriptor are assigned as follows:

8 bits	1 bit	7 bits
Command ID	Read/Write Flag (0 = write, 1 = read)	Data Length (in Bytes)

The MSB of the descriptor is on the left (highest bit of the command ID) and the LSB of the descriptor is on the right (lowest bit of the data length).

DATA Data field
Size = Number of bytes indicated in the Data Length portion of the descriptor.

BCC Block check character
Size = 1 Byte
The block check character is the exclusive-or sum (XOR sum) of the bytes in the descriptor field and the data field.

ETX Identifies the end of the frame text
Size = 1 Byte
(The value of the ETX byte is always 0x03)

ACK/NAK Response Positive frame acknowledge/negative frame acknowledge

Size = 1 byte

(The value for a positive frame acknowledgement is 0x06 and for a negative frame acknowledgement is 0x15.)

All values are formatted as little endian (Intel format).

4.2.2 Error Checking

4.2.2.1 ACK/NAK

When the camera receives a frame, it checks the order of the bytes in the frame and checks to see if the XOR sum of the bytes in the descriptor and the data fields matches the block check character. The camera also checks to see if the number of bytes in the data field is equal to the number specified in the descriptor.

If all checks are correct, an ACK is send to the host. If any check is incorrect, a NAK is sent.

4.2.2.2 Time-outs

Byte Time-out

The camera checks the time between the receipt of each byte in the frame. If the time between any two bytes exceeds 1 second, the camera enters a “garbage state” and discards any more incoming bytes. The camera remains in this state until it sees 1.5 seconds of silence. Once the camera sees 1.5 seconds of silence, it goes into an idle state (looking for an STX).

4.2.2.3 Read Command

In the normal case, when a read command is sent to the camera, the camera responds with an ACK and a frame. The frame will contain the data requested in the read command.

If the camera receives a read command with an unknown command ID in the descriptor, it will respond with an ACK but will not send a frame.

If the host sends a read command and gets no ACK/NAK, the host can assume that no camera is present.

If the host sends a read command and gets an ACK/NAK but does not receive a frame within 500 ms, the host can assume that there was a problem with the read command.

4.2.2.4 Write Command

In the normal case, when a write command is sent to the camera, the camera responds with an ACK.

If the camera receives a write command with an unknown command ID in the descriptor, it will respond with an ACK but will not perform the write.

After a write command has been issued by the host, the host can verify the write by issuing a corresponding read command and checking that the returned data is as expected. The host can also issue a camera status read command (see section 4.2.8) and check the returned data to see if an error condition has been detected.

For many of the write commands listed in the Tables on pages 5-4-11 through 5-4-31, only data within a specified range or a specified group of values is valid. The camera **does not** perform a check to see if the data in the write command is within the allowed range or specified group of allowed values.

4.2.3 Example Commands

4.2.3.1 Read Command

An example of the command message used to read the camera status is:

```
0x02, 0x43, 0x82, 0xC1, 0x03
```

`0x02` - is the STX. The STX is always `0x02`.

`0x43` - is the first byte of the descriptor. The first byte of the descriptor is the command ID. Command IDs can be found in the tables on pages 4-11 through 4-32. If you check the table on page 4-30, you will find that the ID for the camera status read command is 0x43.

`0x82` - is the second byte of the descriptor. The MSB in this byte represents the read/write flag and since this is a read command, the bit should be set to a 1. The other seven bits of this byte represent the data size (in bytes) that will be transferred using this command. If you check the table on page 4-30, the data size for the camera status command is 2 bytes. So the arrangement of the bits in the second byte of the descriptor should be 1000 0010 which translates to 0x82.

Note that for read commands, the data size specified in the descriptor represents the number of bytes of data that you expect to see in the response. No data bytes are actually included in the read command.

`0xC1` - is the block check character (BCC). See page 4-10 for instructions on calculating a BCC.

`0x03` - is the ETX. The ETX is always 0x03.

4.2.3.2 Write Command

An example of the command message used to copy the Work Set into User Set 2 is:

```
0x02, 0x46, 0x01, 0x02, 0x45, 0x03
```

`0x02` - is the STX. The STX is always 0x02.

`0x46` - is the first byte of the descriptor. If you check the table on page 4-28, you will find that the ID for the command to copy the Work Set into a User Set is 0x46.

`0x01` - is the second byte of the descriptor. The MSB in this byte represents the read/write flag and since this is a write command, the bit should be set to a 0. The other seven bits of this byte represent the data size (in bytes) that will be transferred using this command. If you check the table on page 4-28, the data size for the copy Work Set to User Set command is 1 byte. So the arrangement of the bits in the second byte of the descriptor should be 0000 0001 which translates to 0x01.

`0x02` - is the data byte. If you check the table on page 4-28, you will find that to copy the Work Set to User Set 2, the data byte must be set to 0x02.

`0x45` - is the block check character (BCC). See page 4-10 for instructions on calculating a BCC.

`0x03` - is the ETX. The ETX is always 0x03.

4.2.3.3 Calculating the Block Check Character

The block check character in any **A500k** command is the exclusive-or sum (XOR sum) of the bytes in the descriptor and the data fields. For the write command example shown in section 4.2.3.2, the block check character is 0x45. Let's consider at how this block check character was calculated.

In this case, we must find the XOR sum of three bytes. This is done by finding the XOR sum of the first two bytes and then by taking the result and finding the XOR sum of the result plus the third byte.

Calculating XOR sums is most easily understood when numbers are shown in their binary form, so in the example calculations shown below, the hexadecimal digits in our command have been converted to binary.

To find the XOR sum of two binary numbers, you add the two digits in each column using the following rules:

If both digits are 0, the result is 0.

If both digits are 1, the result is 0.

If one of the digits is a 1 and the other is a 0, the result is 1.

With all of this in mind, here is how the check digit for the write command shown in section 4.2.3.2 would be calculated:

```
0 1 0 0  0 1 1 0 = the binary representation of 0x46
0 0 0 0  0 0 0 1 = the binary representation of 0x01
0 1 0 0  0 1 1 1 = the XOR sum of the first two bytes

0 1 0 0  0 1 1 1 = The XOR sum of the first two bytes
0 0 0 0  0 0 1 0 = the binary representation of 0x02
0 1 0 0  0 1 0 1 = The XOR sum

0 1 0 0  0 1 0 1 = 0x45 = the block check character
```

4.2.4 Commands for Setting Camera Parameters

4.2.4.1 Exposure Time Control Mode

Purpose:	To set the exposure time control mode or to read the current exposure time control mode setting. See section 3.2 for an explanation of exposure time control modes.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA0	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0xA0	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0xA0	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	An ID that specifies the exposure mode (see the table below).		

ID	Exposure Time Control Mode
0x00	Free-run, Programmable
0x04	ExSync, Level-controlled
0x05	ExSync, Programmable
0x06	ExSync, Edge-controlled
0x08	Free-run, VGA (A504k/kc only)

4.2.4.2 Timer 1

Purpose:	To set Timer 1 or to read the current Timer 1 setting. Timer 1 is used when the camera is operating in ExSync programmable mode or in free-run mode. See section 3.2 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA6	R/W-Flag 1	Data Length 3	Data -
Response:	Cmd-ID 0xA6	R/W-Flag 0	Data Length 3	Data 3 Bytes
Write Command:	Cmd-ID 0xA6	R/W-Flag 0	Data Length 3	Data 3 Bytes
Response:	None			
Data Format:	Byte 1	Low byte of the Timer 1 setting		
	Byte 2	Mid byte of the Timer 1 setting		
	Byte 3	High byte of the Timer 1 setting		
Data Range:	The timer 1 setting can range from 0x00000A to 0xFFFFFF µs. The recommended maximum value is 0x0080E8 (33ms).			

4.2.4.3 Timer 2

Purpose:	To set Timer 2 or read the current Timer 2 setting. Timer 2 is used when the camera is operating in free-run mode. See section 3.2 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA7	R/W-Flag 1	Data Length 3	Data -
Response:	Cmd-ID 0xA7	R/W-Flag 0	Data Length 3	Data 3 Bytes
Write Command:	Cmd-ID 0xA7	R/W-Flag 0	Data Length 3	Data 3 Bytes
Response:	None			
Data Format:	Byte 1	Low byte of the Timer 2 setting		
	Byte 2	Mid byte of the Timer 2 setting		
	Byte 3	High byte of the Timer 2 setting		
Data Range:	The timer 2 setting can range from 0x000003 to 0xFFFFFF µs.			

4.2.4.4 Long Exposure Compensation (A504k/kc, A503k Only)

Purpose:	To set long exposure compensation or read the current long exposure compensation setting. See section 3.4 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xBD	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0xBD	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0xBD	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	Low byte of the Long Exposure Compensation setting		
	Byte 2	High byte of the Long Exposure Compensation setting		
Data Range:	The Long Exposure Compensation setting can range from 0x46 to 0xA0.			

4.2.4.5 Gain

Purpose:	To set the gain (ADCref) or to read the current gain (ADCref) setting. See section 3.7 for more information on gain.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0x80	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x80	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0x80	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	Gain setting		
Data Range:	The gain setting can range from 0x00 to 0xFF. See the restrictions described in section 3.7.			

4.2.4.6 Negative Offset

Purpose:	To set the negative offset or to read the current negative offset setting. If you use OfsNeg, set OfsPos to 0. See section 3.7 for more information on offset.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0x84	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x84	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0x84	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	Negative offset setting		
Data Range:	The negative offset setting can range from 0x00 to 0xFF.			

4.2.4.7 Positive Offset

Purpose:	To set the positive offset or to read the current positive offset setting. If you use OfsPos, set OfsNeg to 0. See section 3.7 for more information on offset.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0x86	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x86	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0x86	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	Negative offset setting		
Data Range:	The positive offset setting can range from 0x00 to 0xFF. Since the offset is mostly negative, we recommend to set this value to 0.			

4.2.4.8 DSNU Constancy and Shutterline Correction Enable (A503k Only)

Purpose: To enable/disable the DSNU constancy feature and/or the shutterline correction feature. See section 3.8 for more information on the DSNU constancy feature and section 3.9 for more information on shutterline correction.

Type: This is a read or write command.

Read Command:	Cmd-ID 0x91	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x91	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0x91	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			

Data Format:

Byte 1 — An ID that specifies the features.
- Bit 0 — Switches the DSNU constancy feature
- Bit 4 — Switches the shutterline correction feature

(see the table below)

ID	DSNU Constancy and Shutterline Correction Features
0x00	DSNU constancy OFF, shutterline correction OFF
0x01	DSNU constancy ON, shutterline correction OFF
0x10	DSNU constancy OFF, shutterline correction ON
0x11	DSNU constancy ON, shutterline correction ON

4.2.4.9 Shutterline Correction (A503k Only)

Purpose:	To set the shutterline correction value. See section 3.9 for more information on shutterline correction.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0x98	R/W-Flag 1	Data Length 3	Data -
Response:	Cmd-ID 0x98	R/W-Flag 0	Data Length 3	Data 3 Bytes
Write Command:	Cmd-ID 0x98	R/W-Flag 0	Data Length 3	Data 3 Bytes
Response:	None			
Data Format:	Byte 1	Gray value to be added to the 10 bit pixel value		
	Byte 2	0x00		
	Byte 3	0x00		
Data Range:	The shutterline correction setting can range from 0 DN (0x000000) to 255 DN (0x0000FF). The default setting is 12 DN (0x00000C)			

4.2.4.10 Digital Shift

Purpose:	To enable or disable digital shift. See section 3.10 for an explanation of digital shift.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA5	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0xA5	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0xA5	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	An ID that specifies the digital shift status (see the table below).		

ID	Digital Shift	
0x00	No digital shift	
0x01	Digital shift once	(multiplies output 2X)
0x02	Digital shift twice	(multiplies output 4X)
0x03	Digital shift by three	(multiplies output 8X)

See section 3.10.2 for precautions that you must consider when using digital shift.

4.2.4.11 Area of Interest Starting Column

Purpose:	To set the left starting column for the area of interest or to read the current starting column setting. See section 3.11 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA9	R/W-Flag 1	Data Length 2	Data -
Response:	Cmd-ID 0xA9	R/W-Flag 0	Data Length 2	Data 2 Bytes
Write Command:	Cmd-ID 0xA9	R/W-Flag 0	Data Length 2	Data 2 Bytes
Response:	None			
Data Format:	Byte 1	Low byte of the starting pixel setting		
	Byte 2	High byte of the starting pixel setting		
Data Range:	The starting column can range from 0x0000 to 0x04F6. It can only be set in multiples of 10. When you set column *n* using this command, the actual starting column will be *n* + 1. For example, if you set the starting column to 0 with this command, the actual starting column = 0 + 1 = 1.			

4.2.4.12 Area of Interest Width in Columns

Purpose:	To set the width in columns for the area of interest or to read the current width setting. See section 3.11 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xAB	R/W-Flag 1	Data Length 2	Data -
Response:	Cmd-ID 0xAB	R/W-Flag 0	Data Length 2	Data 2 Bytes
Write Command:	Cmd-ID 0xAB	R/W-Flag 0	Data Length 2	Data 2 Bytes
Response:	None			
Data Format:	Byte 1	Low byte of the length in pixel setting		
	Byte 2	High byte of the length in pixel setting		
Data Range:	The width in columns can range from 0x000A to 0x0500. The width can only be set in multiples of 10 (A504k/kc, A501k/kc) or 40 (A503k).			

4.2.4.13 Area of Interest Starting Line

Purpose:	To set the starting line for the Area of Interest or to read the current starting pixel setting. See section 3.11 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA8	R/W-Flag 1	Data Length 2	Data -
Response:	Cmd-ID 0xA8	R/W-Flag 0	Data Length 2	Data 2 Bytes
Write Command:	Cmd-ID 0xA8	R/W-Flag 0	Data Length 2	Data 2 Bytes
Response:	None			
Data Format:	Byte 1	Low byte of the starting pixel setting		
	Byte 2	High byte of the starting pixel setting		
Data Range:	The starting line setting can range from 0x0000 to 0x03FF. For color cameras, it can only be set in steps of 2. **(Note that the starting pixel = *n* +1 where *n* is the value of the starting pixel setting.)**			

4.2.4.14 Area of Interest Height in Lines

Purpose:	To set the height in lines for the Area of Interest or to read the current height setting. See section 3.11 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xAA	R/W-Flag 1	Data Length 2	Data -
Response:	Cmd-ID 0xAA	R/W-Flag 0	Data Length 2	Data 2 Bytes
Write Command:	Cmd-ID 0xAA	R/W-Flag 0	Data Length 2	Data 2 Bytes
Response:	None			
Data Format:	Byte 1	Low byte of the length in pixel setting		
	Byte 2	High byte of the length in pixel setting		
Data Range:	The height in lines setting can range from 0x0002 to 0x0400. For color cameras, the height can only be set in steps of 2 starting at 0x0002.			

4.2.4.15 Area of Interest Stamp and Dynamic Area of Interest (A504k/kc, A503k Only)

Purpose:	To activate or deactivate the Area of Interest Stamp and Dynamic Area of Interest or to read the settings. See sections 3.11.3 and 3.11.2 for details.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0x99	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x99	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0x99	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	An ID that specifies whether AOI Stamp and Dynamic AOI are acivated or deactivated (see the table below).		

ID	Setting
0x00	AOI Stamp and Dynamic AOI deactivated (standard mode)
0x40	AOI Stamp deactivated and Dynamic AOI activated
0x80	AOI Stamp activated and Dynamic AOI deactivated
0xC0	AOI Stamp and Dynamic AOI activated

4.2.4.16 FlashCtrl: Flash Trigger Modes

Purpose: To set the flash trigger mode or to read the current flash trigger mode setting. See sections 2.1.4 and 2.5.8 for an explanation of flash trigger modes.

Type: This is a read or write command.

Read Command:	Cmd-ID 0xAC	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0xAC	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0xAC	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			

Data Format: Byte 1 — An ID that specifies the flash control mode (see the table below).

ID	Flash Trigger Mode (standard TTL, push/pull driver)
0x00	The FlashOut signal is always low
0x01	The FlashOut signal is high while the internal Integrate Enabled signal is high.
0x02	The FlashOut signal is high while the ExFlash signal from the framegrabber. is high
0x03	The FlashOut signal is always high
0x05	The FlashOut signal is low while the internal Integrate Enabled signal is high.
0x06	The FlashOut signal is low while the ExFlash signal from the framegrabber. is high

ID	Advanced modes to combine with the upper modes:
0x10	Open collector or Low Side Switch, 5 V max
0x20	High Side Switch 5 V

To combine an advanced mode with a flash trigger mode, add the hexadecimal number of the advanced code and the one of the flash trigger mode together.

You can not select Low Side Switch and High Side Switch at the same time.

4.2.5 Test Image Command

Purpose:	To enable or disable a test image, and to select a test image. See section 3.12 for an explanation of the available test images.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA1	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0xA1	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0xA1	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	An ID that specifies the test image (see the table below).		

ID	Test Image
0x00	Image from sensor (standard mode)
0x01	Gray Gradient Test Image
0x02	Color Gradient Test Image (Bayer pattern)
0x03	Running Line Test Image
0x04	White Screen Test Image

4.2.6 Query Commands

4.2.6.1 Read Vendor Information

Purpose:	To read the camera vendor's name.			
Type:	This is a read only command.			
Read Command:	Cmd-ID 0x01	R/W-Flag 1	Data Length 16	Data -
Response:	Cmd-ID 0x01	R/W-Flag 0	Data Length 16	Data 16 Bytes
Data Format:	Zero terminated string if less than 16 bytes are needed for the vendor information. Unterminated string if all 16 bytes are needed.			

4.2.6.2 Read Model Information

Purpose:	To read the camera's model number.			
Type:	This is a read only command.			
Read Command:	Cmd-ID 0x02	R/W-Flag 1	Data Length 16	Data -
Response:	Cmd-ID 0x02	R/W-Flag 0	Data Length 16	Data 16 Bytes
Data Format:	Zero terminated string if less than 16 bytes are needed for the model information. Unterminated string if all 16 bytes are needed.			

4.2.6.3 Read Product ID

Purpose:	To read the camera's product ID number.			
Type:	This is a read only command.			
Read Command:	Cmd-ID 0x03	R/W-Flag 1	Data Length 16	Data -
Response:	Cmd-ID 0x03	R/W-Flag 0	Data Length 16	Data 16 Bytes
Data Format:	Zero terminated string if less than 16 bytes are needed for the product ID information. Unterminated string if all 16 bytes are needed.			

4.2.6.4 Read Serial Number

Purpose:	To read the camera's serial number.			
Type:	This is a read only command.			
Read Command:	Cmd-ID 0x04	R/W-Flag 1	Data Length 16	Data -
Response:	Cmd-ID 0x04	R/W-Flag 0	Data Length 16	Data 16 Bytes
Data Format:	Zero terminated string if less than 16 bytes are needed for the serial number information. Unterminated string if all 16 bytes are needed.			

4.2.6.5 Read Camera Version

Purpose:	To read the camera version information.		
Type:	This is a read only command.		
Read Command:	Cmd-ID 0x05	R/W-Flag 1	Data Length 3	Data -
Response:	Cmd-ID 0x05	R/W-Flag 0	Data Length 3	Data 3 Bytes
Data Format:	Byte 1	Low Byte of firmware version		BCD coded
	Byte 2	High Byte of firmware version		BCD coded
	Byte 3	Register Layout ID		

4.2.6.6 Read EEPROM Firmware Version

Purpose:	To read the EEPROM firmware version information.		
Type:	This is a read only command.		
Read Command:	Cmd-ID 0x06	R/W-Flag 1	Data Length 3	Data -
Response:	Cmd-ID 0x06	R/W-Flag 0	Data Length 3	Data 3 Bytes
Data Format:	Byte 1	Low byte of firmware version		BCD coded
	Byte 2	High byte of firmware version		BCD coded
	Byte 3	Register Layout ID		

4.2.6.7 Read Microcontroller Firmware Version

Purpose:	To read the microcontroller firmware version.			
Type:	This is a read only command.			
Read Command:	Cmd-ID 0x40	R/W-Flag 1	Data Length 3	Data -
Response:	Cmd-ID 0x40	R/W-Flag 0	Data Length 3	Data 3 Bytes
Data Format:	Byte 1	Low byte of firmware version		BCD coded
	Byte 2	High byte of firmware version		BCD coded
	Byte 3	Register Layout ID		

4.2.6.8 Read FPGA Firmware Version

Purpose:	To read the FPGA firmware version.			
Type:	This is a read only command.			
Read Command:	Cmd-ID 0x41	R/W-Flag 1	Data Length 3	Data -
Response:	Cmd-ID 0x41	R/W-Flag 0	Data Length 3	Data 3 Bytes
Data Format:	Byte 1	Low byte of firmware version		BCD coded
	Byte 2	High byte of firmware version		BCD coded
	Byte 3	Register Layout ID		

4.2.6.9 Read Temperature

Purpose:	To read the camera's temperature. The temperature is measured on the inner PCB.			
Type:	This is a read only command.			
Read Command:	Cmd-ID 0x70	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x70	R/W-Flag 0	Data Length 1	Data 1 Byte
Data Format:	The result is given in °C as 8 bit signed number.			

4.2.7 Commands for Manipulating Configuration Sets

4.2.7.1 Copy the Factory Set or the User Set into the Work Set (Profile Load)

Purpose: To copy the Factory Set or one of the 15 User Sets into the Work Set. See section 3.13 for an explanation of configuration sets.

The write command will cause the selected set to be copied into the Work Set and the set will become active immediately. Write commands greater than 0x0F will be ignored.

The read command returns the ID of the set that was last copied into the Work Set. (If nothing has been copied to the Work Set since the last power up or reset, the read command will return the ID for "no active set." This condition indicates that no valid Factory Set or User Sets were found. It will also cause the orange LED on the back of the camera to show six flashes.)

Type: This is a read or write command.

Read Command:	Cmd-ID 0x45	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x45	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0x45	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			

Data Format: Byte 1 — An ID that specifies the set. (see the table below).

Set ID	Set
0x00	Factory Set
0x01	User Set 1
0x02	User Set 2
0x03	User Set 3
0x04	User Set 4
0x05	User Set 5
0x06	User Set 6
0x07	User Set 7
0x08	User Set 8
0x09	User Set 9
0x0A	User Set 10
0x0B	User Set 11
0x0C	User Set 12
0x0D	User Set 13
0x0E	User Set 14
0x0F	User Set 15
0xFF	No active set

4.2.7.2 Copy the Work Set into a User Set (Profile Save)

Purpose:	To copy the Work Set into one of the 15 User Sets. See section 3.13 for an explanation of configuration sets.			
Type:	This is a write only command.			
Write Command:	Cmd-ID 0x46	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	An ID that specifies the user set. (see the table below).		

Set ID	Set
0x01	User Set 1
0x02	User Set 2
0x03	User Set 3
0x04	User Set 4
0x05	User Set 5
0x06	User Set 6
0x07	User Set 7
0x08	User Set 8
0x09	User Set 9
0x0A	User Set 10
0x0B	User Set 11
0x0C	User Set 12
0x0D	User Set 13
0x0E	User Set 14
0x0F	User Set 15

4.2.7.3 Select the Startup Pointer (Profile Startup)

Purpose: The Startup Pointer is used to tag the configuration set that will be copied into the Work Set at power on (see section 3.13).

The write command is used to set the Startup Pointer to the Factory Set or to one of the User Sets.

The read command returns the Set ID for the current setting.

Type: This is a read or write command.

Read Command:	Cmd-ID 0x47	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0x47	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0x47	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			

Data Format: Byte 1 — An ID that specifies the set. (see the table below).

Set ID	Set
0x00	Factory Set
0x01	User Set 1
0x02	User Set 2
0x03	User Set 3
0x04	User Set 4
0x05	User Set 5
0x06	User Set 6
0x07	User Set 7
0x08	User Set 8
0x09	User Set 9
0x0A	User Set 10
0x0B	User Set 11
0x0C	User Set 12
0x0D	User Set 13
0x0E	User Set 14
0x0F	User Set 15

4.2.8 Camera Status Command

Purpose: The camera has been programmed to detect several error conditions. When an error condition is detected, a flag is set. The status command allows you to read the error flags.

Type: This is a read only command.

	Cmd-ID	R/W-Flag	Data Length	Data
Read Command:	0x43	1	2	-
Response:	0x43	0	2	2 Bytes

Data Format:

Byte 1: Each bit specifies an error condition (see table below). If a bit is set to 1, the error condition assigned to that bit is present. If the bit is set to 0, the error is not present.

Byte 2: Each bit specifies an error condition (see table below). If a bit is set to 1, the error condition assigned to that bit is present. If the bit is set to 0, the error is not present.

Byte 1	
Bit 0	No ExSync signal in the last 5 seconds
Bit 1	A reset has occurred.
Bit 2	The camera is unlocked
Bit 3	Reserved
Bit 4	Unknown command ID specified in a read or write command
Bit 5	A read or write command could not be executed; access denied
Bit 6	The length member of the last command does not match the defined length
Bit 7	Parameter error

Byte 2	
Bit 0	FPGA; general error
Bit 1	FPGA; no FPGA firmware available
Bit 2	No FPGA/ADC command list available
Bit 3	Error in FPGA/ADC command list item
Bit 4	User set is erroneous
Bit 5	Factory set is erroneous
Bit 6	EEPROM checksum error (this is a checksum used to determine if the contents of the EEPROM are valid)
Bit 7	No EEPROM command list available

4.2.9 Bitrate Command

Purpose:	To set the bitrate of the serial communications link. The bitrate is changed immediately after the successful receipt of this command. (The default bitrate is 9600.)			
Type:	This is a write only command.			
Write Command:	Cmd-ID 0x44	R/W-Flag 0	Data Length 4	Data 4 Bytes
Response:	None			

Data Format:

Byte 1	An ID that specifies the bitrate (see table below).
Byte 2	undefined - always write 0x00
Byte 3	undefined - always write 0x00
Byte 4	undefined - always write 0x00

ID	Bitrate
0x12	4800
0x13	9600
0x14	14400
0x15	19200
0x17	38400
0x19	57600
0x1A	76800
0x1B	115200

When changing the bitrate for serial communication, use the following procedure:

1. Issue the write command with the new bitrate.
2. Wait one second.
3. Change the bitrate on the serial port that the camera is using:
   a) If you are using a Camera Link frame grabber, change the bit rate on the frame grabber's RS-644 serial port.
   b) If you are using the camera with a k-BIC, change the bit rate on your PC's RS-232 serial port (**A501k/kc** only).
4. Resume communication.

Notes: At a camera reset or a power off/on, the camera will return to the 9600 bps default setting.

The RS-644 serial port on some Camera Link frame grabbers will only support a bitrate of 9600. If you are using a Camera Link frame grabber, check the grabber's documentation before attempting to change the bitrate.

4.2.10 Camera Reset Command

Purpose:	Initiates a camera reset. The behavior is similar to a power up reset.			
Type:	This is a write only command.			
Write Command:	Cmd-ID 0x42	R/W-Flag 0	Data Length 2	Data 2 Bytes
Response:	None			
Data Format:	Byte 1	Low byte	0xCF is always used	
	Byte 2	High byte	0x07 is always used	

4.2.11 Power Control Command

Purpose:	To set the camera to standby mode or to fully functional mode. See section 2.9 on power up time.			
Type:	This is a read or write command.			
Read Command:	Cmd-ID 0xA2	R/W-Flag 1	Data Length 1	Data -
Response:	Cmd-ID 0xA2	R/W-Flag 0	Data Length 1	Data 1 Byte
Write Command:	Cmd-ID 0xA2	R/W-Flag 0	Data Length 1	Data 1 Byte
Response:	None			
Data Format:	Byte 1	An ID that specifies the power mode (see the table below).		

ID	Power Mode
0x00	Camera in standby
0x01	Camera fully functional

5 Mechanical Considerations

5.1 Camera Dimensions and Mounting Facilities

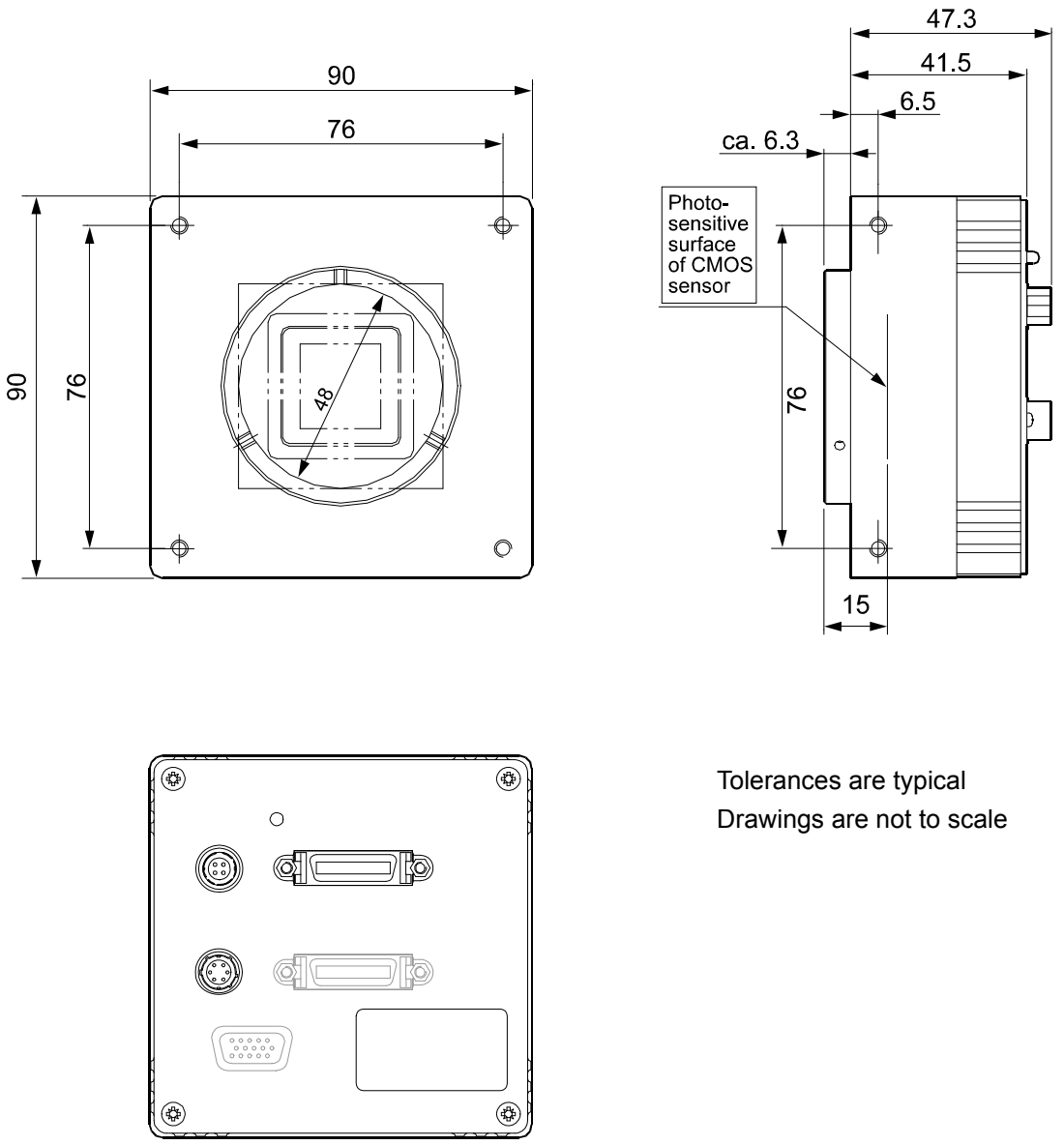
The **A500k** camera housing is manufactured with high precision. Planar, parallel, and angular sides guarantee precise mounting with high repeatability.

A500k cameras are equipped with four M4 mounting holes on the front and two M4 mounting holes on each side as indicated in Figure 5-1.

A tripod mount is availabe as an option. The Basler part number is 1000014110.

Caution!

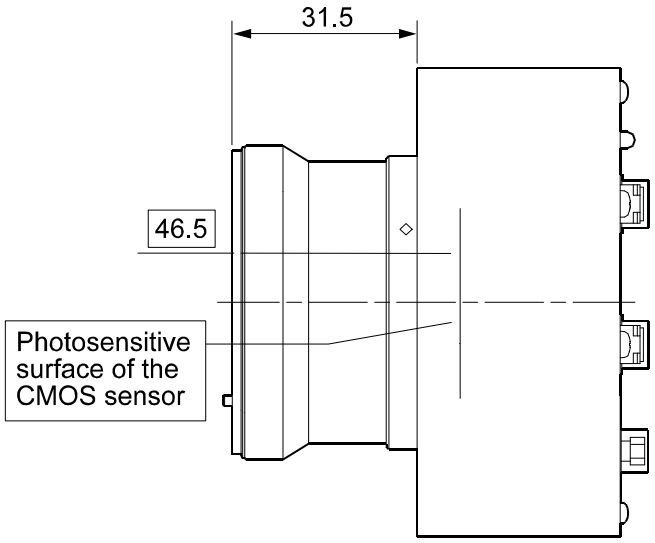
To avoid collecting dust on the sensor, mount a lens on the camera immediately after unpacking it.



Tolerances are typical
Drawings are not to scale

Figure 5-1: **A500k** Mechanical Dimensions (in mm)

5.2 F-Mount Adapter Dimensions



Drawing is not to scale

Figure 5-2: F-Mount Adapter Dimensions (in mm)

5.3 Positioning Accuracy of the Sensor Chip

Positioning accuracy of the sensor chip is as shown in Figure 5-3.

Since the translatory and rotational positioning tolerance depend on each other, the maximum rotational mis-positioning and the maximum horizontal/vertical mis-positioning cannot occur at the same time.

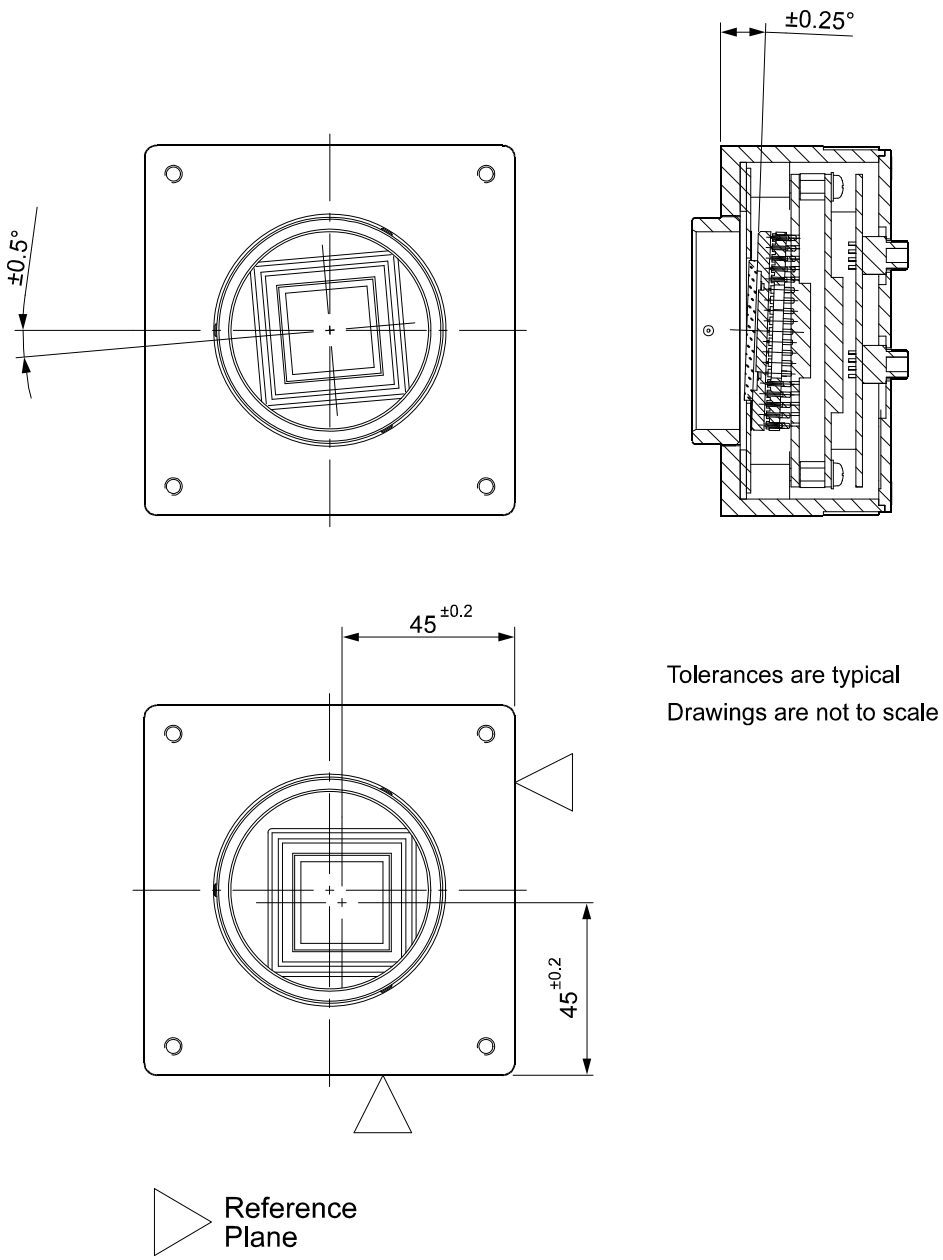


Figure 5-3: Sensor Positioning Accuracy (in mm or Degrees)

5.4 Mechanical Stress Test Results

Cameras were submitted to an independent mechanical testing laboratory and subjected to the stress tests listed below. The mechanical stress tests were performed on selected camera models with standard housings. After mechanical testing, the cameras exhibited no detectable physical damage and produced normal images during standard operational testing.

Test	Standard	Conditions
Vibration (sinusoidal, each axis)	DIN IEC 60068-2-6	5-8.5 Hz / 1.5 mm_8.5-150 Hz / 10 m/s^2_1 Octave/Minute 5 repetitions (00:25 h test period)
Shock (each axis)	DIN IEC 60068-2-27	C 11 ms / 3 shocks / positive 100 m/s^2 11 ms / 3 shocks / negative
Bump (each axis)	DIN IEC 60068-29	100 m/s^2 11 ms / 100 shocks / positive 100 m/s^2 11 ms / 100 shocks / negative

Table 5-1: Mechanical Stress Tests

6 Troubleshooting and Support

6.1 Troubleshooting

6.1.1 Fault Finding Using the Camera's LED

A500k cameras regularly perform self tests. Detected errors are signaled by flashes of the LED on the back of the camera. The number of flashes indicates the detected error. If several error states are present, the LED outputs the error codes in succession.

See Table 6-1 for the description of the flashes and the error states.

LED	Description
Orange and on Continuous	The camera has power and is OK.
3 flashes	ExSync has not changed state for 5 seconds or longer. If you are not supplying an ExSync signal to the camera, this is a normal condition and should be ignored. Otherwise check the cable and the ExSync generating device.
5 flashes	The Work Set could not be stored into a User set. Contact Basler support.
6 flashes	A User Set or the Factory Set could not be loaded into the Work Set. Contact Basler support.
7 flashes	A valid list of commands was not available. Contact Basler support.
8 flashes	The FPGA could not be configured. Contact Basler Support

Table 6-1: Camera Status Indicators

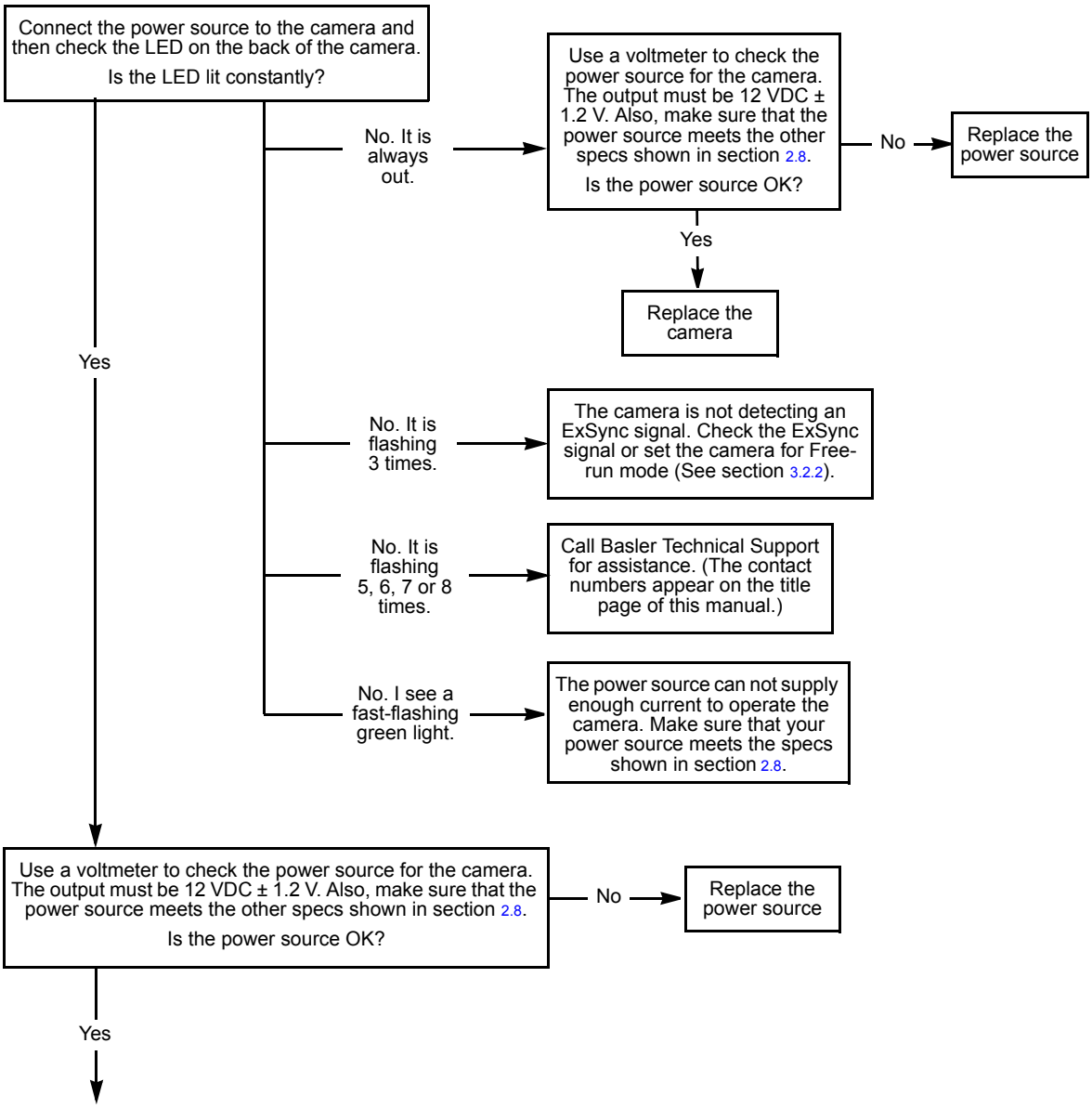
6.1.2 Troubleshooting Charts

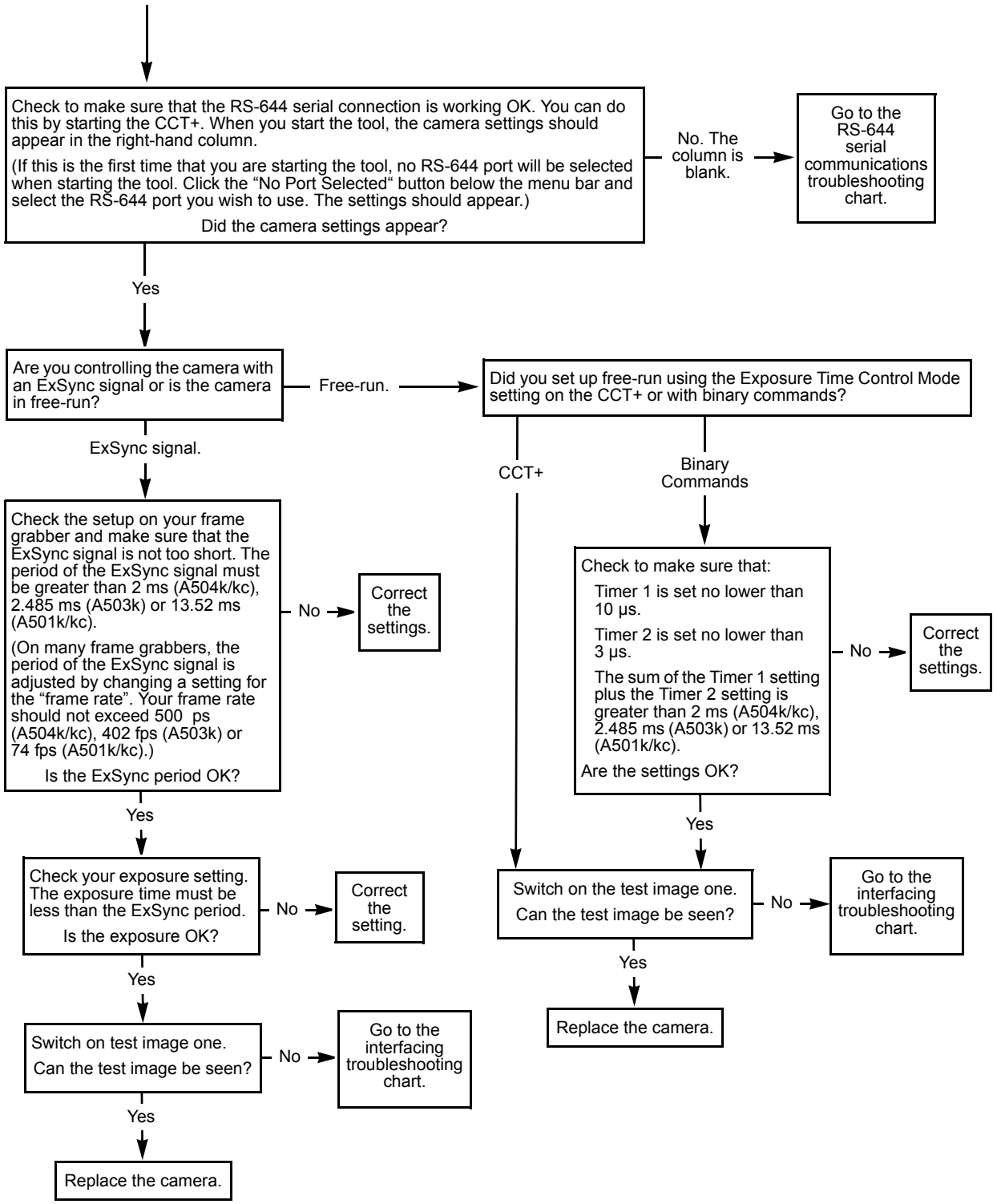
The following pages contain several troubleshooting charts which can help you find the cause of problems that users sometimes encounter. The charts assume that you are familiar with the camera's features and settings and with the settings for your frame grabber. If you are not, we suggest that you review the manuals for your camera and frame grabber before you troubleshoot a problem.

6.1.2.1 No Image

Use this chart if you see no image at all when you attempt to capture an image with your frame grabber (in this situation, you will usually get a message from the frame grabber such as "time-out"). If you see a poor quality image, a completely black image, or a completely white image, use the chart in section 6.1.2.2.

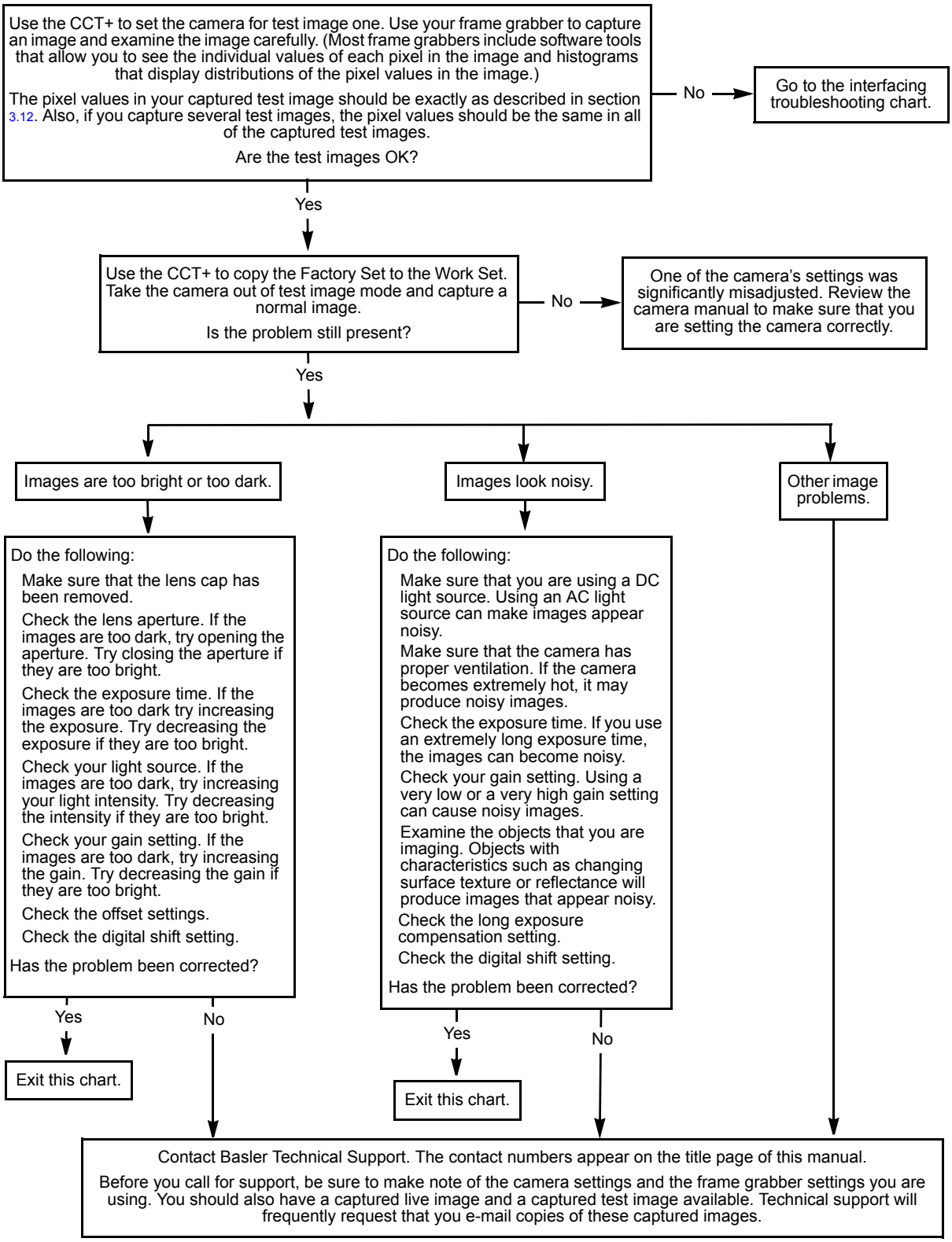
Always switch off power to the system before making or breaking any connection.




Check to make sure that the RS-644 serial connection is working OK. You can do this by starting the CCT+. When you start the tool, the camera settings should appear in the right-hand column.
(If this is the first time that you are starting the tool, no RS-644 port will be selected when starting the tool. Click the “No Port Selected“ button below the menu bar and select the RS-644 port you wish to use. The settings should appear.)
Did the camera settings appear?
No. The column is blank.
Go to the RS-644 serial communications troubleshooting chart.
Yes
Are you controlling the camera with an ExSync signal or is the camera in free-run?
Free-run.
Did you set up free-run using the Exposure Time Control Mode setting on the CCT+ or with binary commands?
ExSync signal.
CCT+
Binary Commands
Check the setup on your frame grabber and make sure that the ExSync signal is not too short. The period of the ExSync signal must be greater than 2 ms (A504k/kc), 2.485 ms (A503k) or 13.52 ms (A501k/kc).
(On many frame grabbers, the period of the ExSync signal is adjusted by changing a setting for the “frame rate”. Your frame rate should not exceed 500 ps (A504k/kc), 402 fps (A503k) or 74 fps (A501k/kc).)
Is the ExSync period OK?
No
Correct the settings.
Check to make sure that:
Timer 1 is set no lower than 10 µs.
Timer 2 is set no lower than 3 µs.
The sum of the Timer 1 setting plus the Timer 2 setting is greater than 2 ms (A504k/kc), 2.485 ms (A503k) or 13.52 ms (A501k/kc).
Are the settings OK?
No
Correct the settings.
Yes
Yes
Check your exposure setting. The exposure time must be less than the ExSync period.
Is the exposure OK?
No
Correct the setting.
Switch on the test image one.
Can the test image be seen?
No
Go to the interfacing troubleshooting chart.
Yes
Yes
Switch on test image one.
Can the test image be seen?
No
Go to the interfacing troubleshooting chart.
Yes
Replace the camera.
Replace the camera.

6.1.2.2 Poor Quality Image

Use this chart if the image is poor quality, is completely white, or is completely black. If you get no image at all when you attempt to capture an image with the frame grabber, use the chart that appears in section 6.1.2.1.

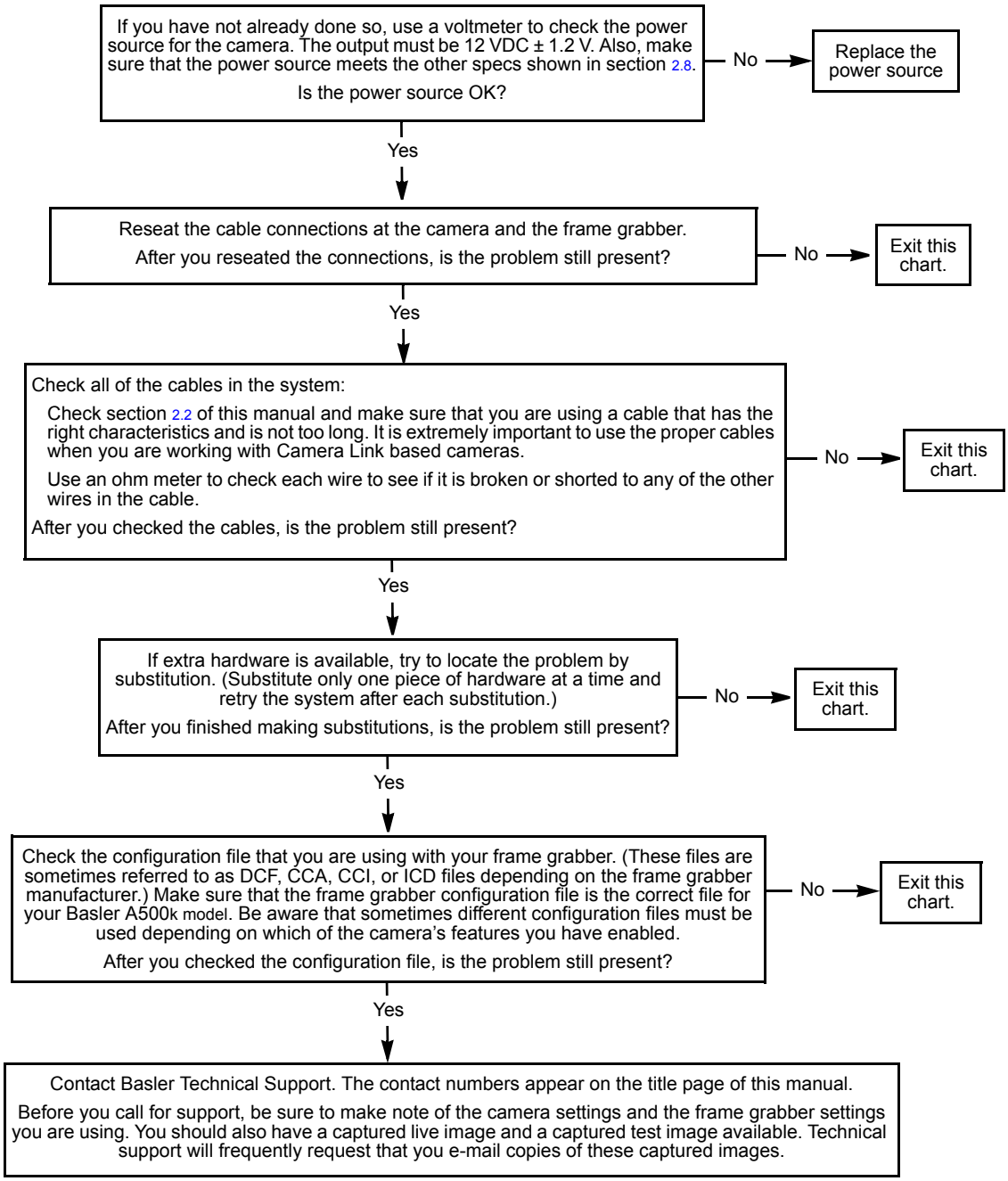


6.1.2.3 Interfacing

Use the interfacing troubleshooting charts if you think that there is a problem with the cables between your devices or if you have been directed here from another chart.

Interfacing Chart

Always switch off power to the system before making or breaking any connection.

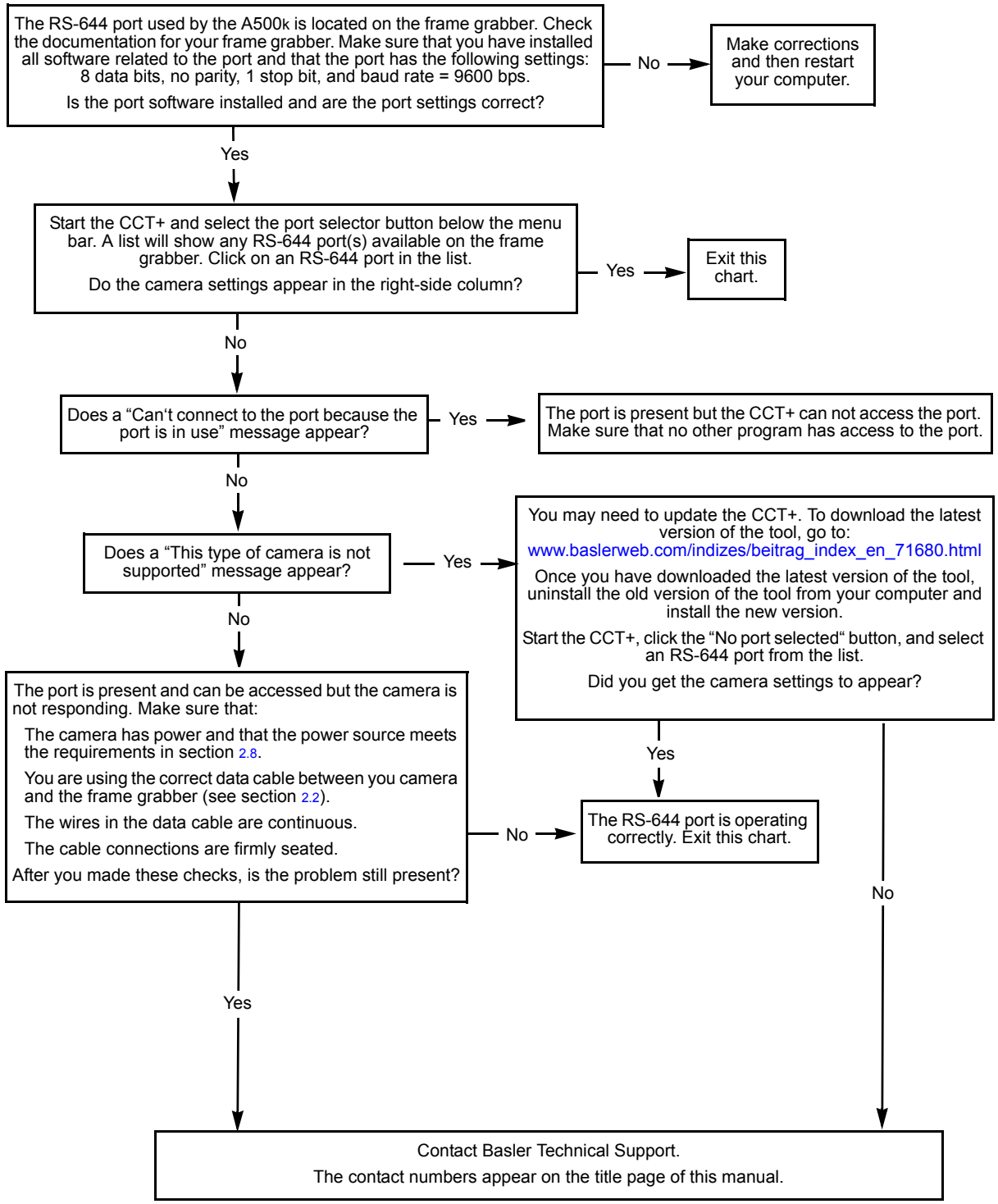


6.1.2.4 RS-644 Serial Communication

Use the serial communication troubleshooting charts if you think that there is a problem with RS-644 serial communication or if you have been directed here from another chart.

Serial Communication Chart (without a k-BIC)

Always switch off power to the system before making or breaking any connection.



6.2 Technical Support

6.2.1 Technical Support Resources

If you need advice about your camera or if you need assistance troubleshooting a problem with your camera, you can contact the Basler technical support team for your area. Basler technical support contact information is located in the front pages of this manual.

You will also find helpful information such as frequently asked questions, downloads, and application notes on the Basler website at:
www.baslerweb.com/indizes/beitrag_index_en_22089.html

6.2.2 Obtaining an RMA Number

Whenever you want to return material to Basler, you must request a Return Material Authorization (RMA) number before sending it back. The RMA number **must** be stated in your delivery documents when you ship your material to us! Please be aware that if you return material without an RMA number, we reserve the right to reject the material.

You can find detailed information about how to obtain an RMA number on the Basler website at:
www.baslerweb.com/beitraege/beitrag_en_79701.html

6.2.3 Before Contacting Basler Technical Support

To help you as quickly and efficiently as possible when you have a problem with a Basler camera, it is important that you collect several pieces of information before you contact Basler technical support.

Copy the form that appears on the next two pages, fill it out, and fax the pages to your local dealer or to your nearest Basler support center. Or, you can send an e-mail listing the requested pieces of information and with the requested files attached. Our Basler technical support contact information is shown in the title section of this manual.

1 The camera's product ID: _____

2 The camera's serial number: _____

3 The operating system: _____

4 Frame grabber that you use with the camera: _____

_____

5 CCT+ version that you use with the camera: _____

_____

6 Describe the problem in as much detail as possible: _____

(If you need more space, use an extra sheet of paper.) _____

_____

_____

_____

_____

7 If known, what's the cause of the problem? _____

_____

_____

8 When did the problem occur? ☐ After start. ☐ While running.

☐ After a certain action (e.g., a change of parameters):

_____

_____

☐ _____

_____

9 How often did/does the problem occur?

- ☐ Once.
- ☐ Every time.
- ☐ Regularly when:

  _____

- ☐ Occasionally when:

  _____

  _____

10 How severe is the problem?

- ☐ Camera can still be used.
- ☐ Camera can be used after I take this action:

  _____

  _____

- ☐ Camera can no longer be used.

11 Did your application ever run without problems?

- ☐ Yes
- ☐ No

12 Parameter set

It is very important for Basler Technical Support to get a copy of the exact camera parameters that you were using when the problem occurred.

To make a copy of the parameters, start the CCT+, select the File menu, and click Dump Current Settings to File. Send the generated file to Basler technical support.

If you cannot access the camera, please try to state the following parameter settings:

- ☐ Video data output mode: _____
- ☐ Exposure time control mode: _____
- ☐ Exposure time: _____
- ☐ Gain: _____
- ☐ Offset: _____

13 Live image/test image

If you are having an image problem, try to generate and save live images that show the problem. Also generate and save test images. Please save the images in BMP format, zip them, and send them to Basler Technical Support.

Revision History

Doc. ID Number	Date	Changes
DA00057001	14 Oct 2002	Initial release covering series production cameras.
DA00057002	07 Jan 2003	The **A501kc** color camera was added to the series. The high and low byte information was added to the AOI stamp. The AOI Stamp and Dynamic AOI register was renamed and is now called the AOI Feature register.
DA00057003	25 Jul 2003	Vibration, shock, and bump specifications were added. FVAL high time in Figure 2-8 and Figure 2-9 was corrected. Figure 2-5 and Table 2-6 were changed. The flash trigger output schematics for open collector and high side switch and explanation were added in Figure 2-4. The explanation on exposure modes in section 3.3 was improved. The minimum AOI height in lines was changed to 2. The responsivity of the sensor changed, and with it the explanation in section 1.3 and the formulas in section 3.7.1. A power supply recommendation was added to section 2.8.
DA00057004	2 Dec 2004	Marked several values in Table 1-1 as typical. In section 5.3, added sensor horizontal and vertical position tolerances referenced to the sides of the camera. Added a Feedback section.
DA00057005	18 Apr 2005	Updated Figure 2-5 and Figure 2-7 in section 2.3. Corrected flash trigger modes in section 4.2.4.16 (the ID for the flash trigger mode “Always high“ is 0x03 and not 0x04). Corrected Write Command and Data Format in section 4.2.10 (the order of the data bytes have been inversed).
DA00057006	4 April 2006	Corrected the address for Singapore in the “Contacting Basler Support” section of the front matter. Corrected a LED supply voltage for the low side switch in Figure 2-4. Corrected the steps and added information about reset behavior in the note box in section 4.2.9. Corrected the tilt angle tolerance in Figure 5-3. Added section 6.2 that describes what to do before calling tech support.
DA00057007	20 Mar 2007	Updated Basler address in the U.S.A. Added storage conditions in section 1.4. Interchanged required pixel clocks between A504k/kc and A501k/kc in section 2.5.2. Replaced FlashOut signal by Integrate Enabled signal in all figures of section 3.3. Augmented explanations in sections 3.3.1 to 3.3.5. Replaced “ExSync signal“ by “internal control signal“ in section 3.3.4. Made minor corrections and additions throughout the manual. Integrated the A503k.

Doc. ID Number	Date	Changes
DA00057008	5 Dec 2008	Updated the addresses and phone numbers on the contact page. Added warning that warranty is void if serial number sticker is removed. Added warnings about disconnecting cables to sections 1.5, 2.1, and 2.8. Corrected the frame rate formula for the A504k/kc in section 3.11.1. Corrected the description of bit 0 and bit 4 in section 4.2.4.8. Added section 5.4 with the mechanical stress test results. Added section 6.2.2 describing where to find information about obtaining an RMA number. Updated all instances of the Basler web address.

Feedback

Your feedback will help us improve our documentation. Please click the link below to access an online feedback form. Your input is greatly appreciated.

http://www.baslerweb.com/umfrage/survey.html

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